TELEDYNE DALSA
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DALSA • 7075 Place Robert-Joncas, Suite 142 • Montreal, Quebec, H4M 2Z2 • Canada
www.teledynedalsa.com

PC2-Vision

User's Manual

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NOTICE

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About Teledyne DALSA
Teledyne DALSA is an international high performance semiconductor and electronics company that designs, develops, manufactures, and markets digital imaging products and solutions, in addition to providing wafer foundry services.
Teledyne DALSA Digital Imaging offers the widest range of machine vision components in the world. From industry-leading image sensors through powerful and sophisticated cameras, frame grabbers, vision processors and software to easy-to-use vision appliances and custom vision modules.

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Troubleshooting

- Offers suggestions for resolving installation or usage problems.

TELEDYNE DALSA Contact Information

- Phone numbers, web site, and important email addresses.

About the Manual

This manual exists in Adobe Acrobat (PDF) and .chm help formats. These formats make full use of hypertext cross-references and include links to the Teledyne DALSA home page on the Internet, accessed using any web browser.

For PC2-Vision specific information, visit the DALSA web site at www.teledynedalsa.com.

This manual applies to both the PCI and PCIe versions of the board.

Using the Manual

File names, directories, and Internet sites will be in bold text
(for example, **image2.bmp**, **c:\IFC**, **http://www.dalsa.com**).

Text that must be entered using the keyboard will be in typewriter-style text
(for example, `c:\temp`).

Menu and dialog actions will be indicated in bold text in the order of the instructions to be executed, with each instruction separated by bullets. For example, going to the **File** menu and choosing **Save** would be written as **File•Save**.

PC2-Vision Board

The PC2-Vision

Overview

Two versions of the PC2-Vision are available; as a PCI version 2.1 or PCI Express compatible plug-in board. Both versions provides image capture for cost sensitive machine vision applications. This manual applies to both versions.

The acquisition circuitry interfaces with standard (RS-170 and CCIR) and non-standard (progressive scan) analog cameras, RGB and dual-channel analog cameras. PC2-Vision makes interfacing with cameras easy by offering fully programmable timing coupled with efficient cabling and a variety of trigger, strobe and asynchronous reset options. To further simplify the integration task, PC2-Vision provides general-purpose parallel I/O capabilities for controlling or monitoring the status of external events.

PC2-Vision provides a very efficient 32-bit PCI or PCI Express interface, which is capable of bus mastering image data directly to a memory destination within the system (that is, system memory or another PCI or PCI Express target, such as VGA). Transfer rates up to 100 MB/second are sustained, depending upon host capabilities. Consequently, images can be transferred to host memory in a fraction of the time acquired. More bandwidth is, therefore, available for other system resources to utilize by minimizing PC2-Vision transfer time on the PCI or PCI Express bus.

PC2-Vision provides a number of interrupt sources such as image acquisition and bus master transfer completion.

PC2-Vision contains 8MB of memory for buffering image data between the camera and the host system. Onboard memory assures that image information is not lost during transfer to system memory due to PCI bus latency issues. The memory is addressed linearly for maximum utilization. Images are grabbed into local memory and then transferred at very high speeds to the host for processing or display.

PC2-Vision is supported by both Sapera LT and IFC. It is also fully supported by the Sapera Image Processing library.

Note: You can install the PC2-Vision device driver for either IFC or for Sapera LT. You cannot use both IFC and Sapera LT at the same time for PC2-Vision.

PC2-Vision Features and Block Diagram

Features

- Half-size PCI or PCI Express form factor
- Six analog video inputs, AC coupled and terminated to 75Ω
- Acquires up to six monochrome or two RGB cameras; simultaneous acquisition up to three genlocked monochrome cameras
- Supports standard RS-170 and CCIR, non-standard progressive cameras and RGB formats
- External Trigger input; synchronizes acquisition to external events
- Resolution up to 2048 x 2048 interlaced or non-interlaced
- Video controls allow brightness and contrast
- Windows® XP, Windows® Vista and Windows 7/8
- 40MHz digitization rate (8-bit)
- Anti-aliasing filters: 6 MHz, 12 MHz or bypass (software selectable)

See "PC2-Vision Specifications" on page 70 for detailed information on PC2-Vision specifications.

Functional Block Diagram

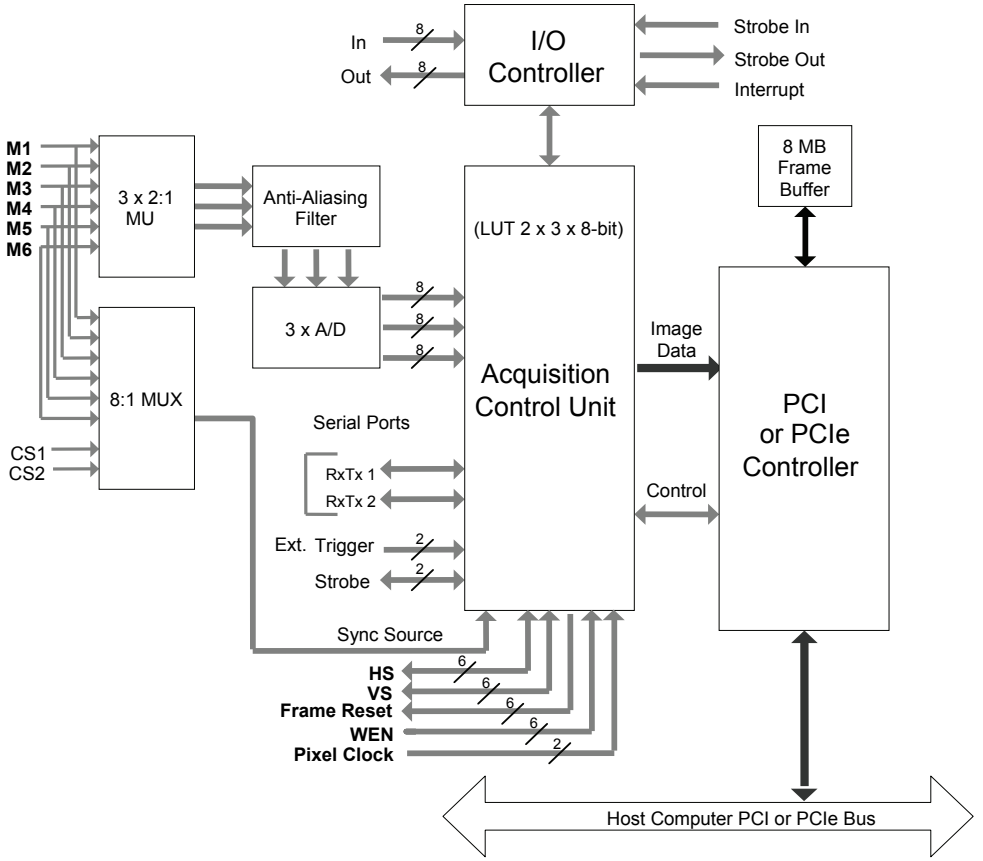


Figure 1: PC2-Vision Block Diagram

Components & Part Numbers

The following table lists the components and part numbers for the PC2-Vision:

Item	Part Number
Board	
PC2-Vision PCI	Contact Sales
PC2-Vision PCI Express	Contact Sales
Cables & Accessories	
Floppy power connector	OC-COMC-POW03
Single camera BNC cable	OC-PC2C-V1B00
Single RGB camera BNC cable	OC-PC2C-V1B01
PCVision Series adapter cable	OC-PC2C-V3A00
Single camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V1H00
Three camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V3H00
Single camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V1H01
Three camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V3H01
Single camera Hirose-12 + Hirose-6 for Jai A-series camera	OC-PC2C-V1H02
Three camera Hirose-12 + Hirose-6 for Jai A-series camera	OC-PC2C-V3H02
Jai CV-M77 RGB camera cable	OC-PC2C-V1D00
Pulnix camera cable (supporting three cameras)	OC-PC2C-V3H03
Jai M-series camera cable (supporting three cameras)	OC-PC2C-V3H04
Parallel I/O connector to female DB25 bracket assembly	4816
Documentation	
PC2-Vision User's manual	OC-PC2M-VUM00

EC & FCC Certificate of Conformity

EC & FCC DECLARATION OF CONFORMITY

We : Teledyne DALSA inc.
7075 Place Robert-Joncas, Suite 142,
St. Laurent, Quebec, Canada, H4M 2Z2

Declare under sole legal responsibility that the following products conform to the protection requirements of council directive 2004/108/EC on the approximation of the laws of member states relating to electromagnetic compatibility:

PC2-Vision

The products to which this declaration relates are in conformity with the following relevant harmonized standards, the reference numbers of which have been published in the Official Journal of the European Communities:

EN55022:2006, A1:2007
EN55024:1998, A1:2001, A2:2003
ENV50204:1995
EN60255-22-4:2002

Further declare under our sole legal responsibility that the product listed conforms to the code of federal regulations CFR 47 part 15 (2008), subpart B, for a class A product.

St. Laurent, Canada — Location
2012-04-09 — Date

Eric Carey, ing.
Director,
Research and Development

Development Software Overview

Sapera++ LT Library

Sapera++ LT is a powerful development library for image acquisition and control. Sapera++ LT provides a single API across all current and future TELEDYNE DALSA hardware. Sapera++ LT delivers a comprehensive feature set including program portability, versatile camera controls, flexible display functionality and management, plus easy to use application development wizards.

Sapera++ LT comes bundled with CamExpert, an easy to use camera configuration utility to create new, or modify existing camera configuration files.

Sapera Processing Library

Sapera Processing is a comprehensive set of C++ classes for image processing and analysis. Sapera Processing offers highly optimized tools for image processing, blob analysis, search (pattern recognition), OCR and barcode decoding.

Installing the PC2-Vision

Warning! (Grounding Instructions)

Static electricity can damage electronic components. Please discharge any static electrical charge by touching a grounded surface, such as the metal computer chassis, before performing any hardware installation.

If you do not feel comfortable performing the installation, please consult a qualified computer technician.

Never remove or install any hardware component with the computer power on. Disconnect the power cord from the computer to disable the power standby mode. This prevents the case where some computers unexpectedly power up when a board is installed.

Upgrading Sapera or any Board Driver

When installing a new version of Sapera or a DALSA acquisition board driver in a computer with a previous installation, the current version **must** be un-installed first. Upgrade scenarios are described below.

Board Driver Upgrade Only

Minor upgrades to acquisition board drivers are typically distributed as ZIP files available in the DALSA web site. Board driver revisions are also available on the next release of the Sapera CD-ROM.

Often minor board driver upgrades do not require a new revision of Sapera. To confirm that the current Sapera version will work with the new board driver:

- Check the new board driver ReadMe file before installing, for information on the minimum Sapera version required.
- If the ReadMe file does not specify the Sapera version, contact TELEDYNE DALSA Technical Support (see "Technical Support" on page 168).

To upgrade the board driver only:

- Logon the computer as an administrator or with an account that has administrator privileges.
- From the Windows start menu select **Start • Control Panel • Add or Remove Programs**.
- Select the DALSA PC2-Vision Device Driver, click **Remove**, and then in the InstallShield dialog click on **Remove** to uninstall the board driver.
- When the driver un-install is complete, reboot the computer.
- Logon the computer as an administrator again.
- Install the new board driver. Run **Setup.exe** if installing manually from a downloaded driver file.
- If the new driver is on a Sapera CD-ROM follow the installation procedure described in the section "Installing PC2-Vision Hardware and Driver" on page 11.
- Note that you can not install a DALSA board driver without Sapera LT installed on the computer.

Sapera and Board Driver Upgrades

When both Sapera and the acquisition board driver are upgraded, follow the procedure described below.

- Logon the computer as an administrator or with an account that has administrator privileges.
- From the Windows start menu select **Start • Control Panel • Add or Remove Programs**.
- Select the DALSA PC2-Vision Device Driver, click **Remove**, and then in the InstallShield dialog click on **Remove** to uninstall the board driver.
- From the Windows start menu select **Start • Control Panel • Add or Remove Programs**.
- Select the DALSA Sapera LT program, click **Remove**, and then in the InstallShield dialog click on **Remove** to uninstall Sapera.
- If prompted to do so, reboot the computer and logon the computer as an administrator again.
- Install the new versions of Sapera and the board driver as if this was a first time installation. For installation procedures, see "Sapera LT Library Installation" on page 11 and "Installing PC2-Vision Hardware and Driver" on page 11 for installation procedures.

Sapera LT Library Installation

Note: to install Sapera LT and the PC2-Vision device driver, logon to the workstation as administrator or with an account that has administrator privileges.

The Sapera LT Development Library (or 'runtime library' if application execution without development is preferred) must be installed before the PC2-Vision device driver.

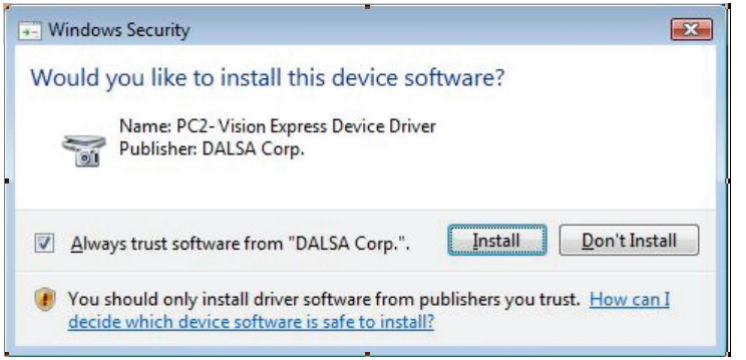
- Insert the TELEDYNE DALSA Sapera CD-ROM. If **AUTORUN** is enabled on your computer, the installation menu is presented.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu and install the required Sapera components.
- The installation program will prompt you to reboot the computer.

Refer to *Sapera LT User's Manual* for additional details about Sapera LT.

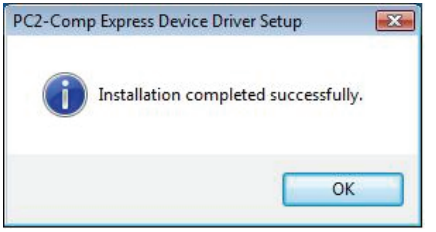
Installing PC2-Vision Hardware and Driver

In a Windows /XP/Vista/7/8 System

- Turn the computer off, disconnect the power cord (disables power standby mode), and open the computer chassis to allow access to the expansion slot area.
- Install the PC2-Vision into a PCI slot or the PCI Express in a x1 expansion slot. The PC2 Express can also be installed in a PCI Express x4, x8 slot, or x16 slots.
- Close the computer chassis and turn the computer on. Driver installation requires administrator rights for the current user of the computer.
- Windows will find the PC2-Vision and start its **Found New Hardware Wizard**. Click on the **Cancel** button to close the Wizard.
- Insert the TELEDYNE DALSA Sapera CD-ROM. If **AUTORUN** is enabled on your computer, the installation menu is presented. Install the PC2-Vision driver.
- If **AUTORUN** is not enabled, use Windows Explorer and browse to the root directory of the CD-ROM. Execute **launch.exe** to start the installation menu. Click **Software Installation**, then **Install Hardware Device Driver**, **Frame Grabbers - Device Drivers,** and **PC2 Series**. Select the **PC2-Vision** board and install the PC2-Vision driver. Note, if you are using Vista with the User Account Control feature enabled, a dialog is displayed when you execute **launch.exe**; click **Allow** to continue with the driver installation.
- Choose the device driver setup type, full installation (required for application development) or runtime installation (supports application execution only).
- When using **Windows XP**, if a message stating that the PC2-Vision software has not passed **Windows Logo testing** is displayed, click on **Continue Anyway** to finish the PC2-Vision driver installation. Reboot the computer if prompted to do so.
- When using **Windows Vista/7/8**, a message asking to install the DALSA device software is displayed. Click **Install**.



- During the installation the PC2-Vision Device Manager firmware loader application starts. Click Update All.
- When the installation is complete, the following dialog box is displayed:



Connecting Camera and Devices

Connector Bracket

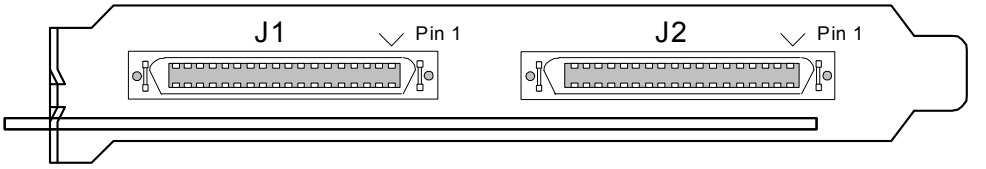


Figure 2: Connector Bracket

There are two MDR (Mini Delta Ribbon) 36-pin female camera connectors on the front bracket of the PC2-Vision board labeled J1 and J2. Both connectors control a group of cameras called ‘channels.’ J1 controls channels 1 to 3. J2 controls channels 4 to 6. Therefore, six monochrome cameras can be connected to the PC2-Vision. See the "PC2-Vision Connector and Jumper Locations" on page 72 for further information.

Note: PC2-Vision's J6 connector must be connected to a floppy power cable to provide 12V to the cameras. Refer to "PC2-Vision component view" on page 72 section for connector locations.

PC2-Vision boards are able to provide up to 500mA of power to the camera from the PCI or PCI Express connector (fused protected). Nonetheless, TELEDYNE DALSA recommends connecting the floppy power connector to ensure sufficient current is driven to the cameras from the PC power supply.

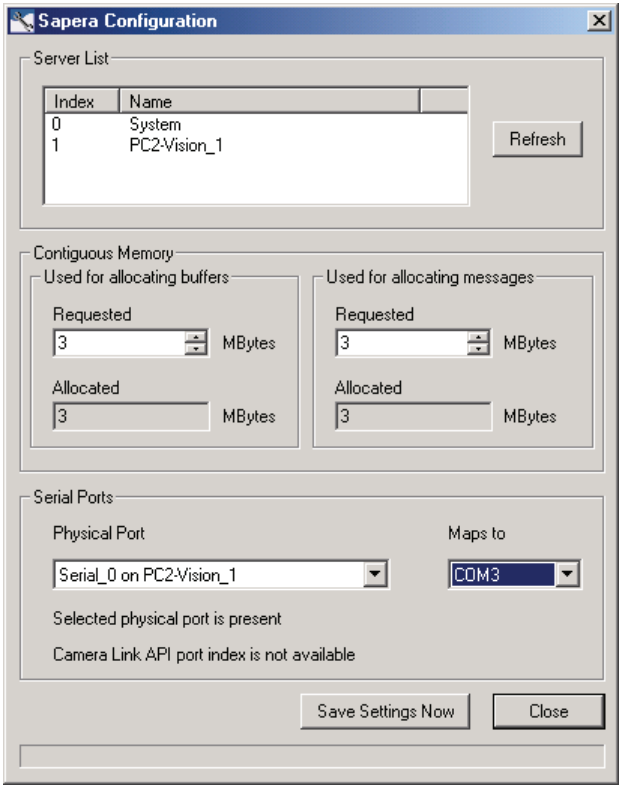
Caution: Sinking more than 500mA from the PC2-Vision PCI or PCI Express connector may result in the auto-reset fuse blowing or in erratic behavior with the camera if it requires more than 500mA. Check your camera datasheet for the required camera current.

Warning: Some cameras have frame reset located on pin 9 of the Hirose-12 connector while other cameras have it on pin 11. It is imperative to use the appropriate camera cable that matches the frame reset pinout. Failure to do so could result in board damage.

COM Port Assignment

The lower section of the Sapera Configuration program screen contains the serial port configuration menu. Configure as follows:

- Open the 'Sapera Configuration' program by selecting **Start•Programs•DALSA•Sapera LT•Sapera Configuration**.
- Use the **Physical Port** drop menu to select the Sapera board device from all available Sapera boards using serial ports (when more then one board is in your system).
- Use the **Maps to** drop menu to assign an available COM number to the Sapera board serial port.
- Click on the **Save Settings Now** button and then the **Close** button. You are prompted to reboot your computer to enable serial port mapping.
- The PC2-Vision serial port (mapped to COM3 in this example) is available as a serial port to any serial port application for camera control. Note that this serial port is not listed in the **Windows•Control Panel•System Properties•Device Manager** because it is a logical serial port mapping.

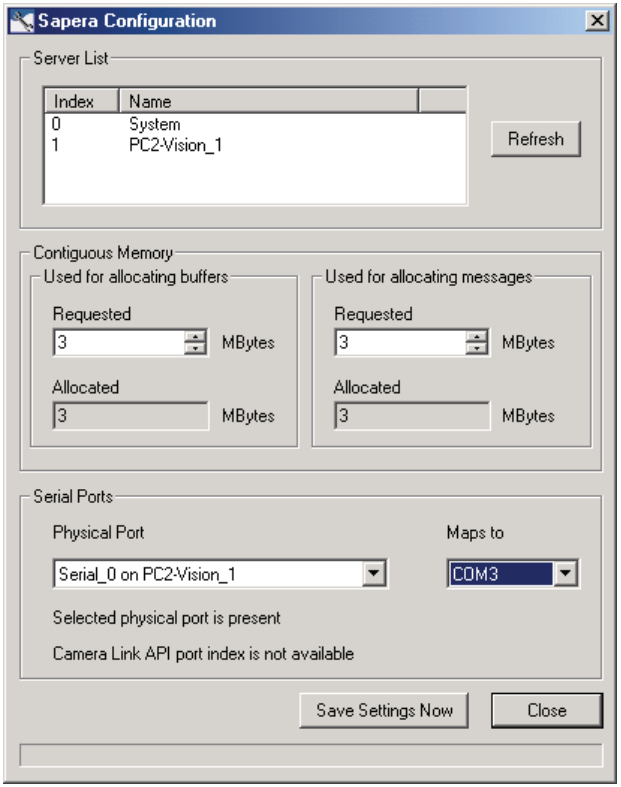


Configuring Sapera

Viewing Installed Sapera Servers

The Sapera Configuration program (**Start•Programs•DALSA•Sapera LT•Sapera Configuration**) allows the user to see all available Sapera servers for the installed Sapera-compatible boards.

The **System** entry represents the system server. It corresponds to the host machine (your computer) and is the only server that should be present at all times. As shown in the following screen image, server index 1 is the PC2-Vision board installed. If required, update the server list by clicking the **Refresh** button.



Increasing Contiguous Memory for Sapera Resources

The **Contiguous Memory** section lets the user specify the total amount of contiguous memory (a block of physical memory occupying consecutive addresses) reserved for the resources needed for **Sapera buffer** allocation and **Sapera messaging**. For both items, the **Requested** value dialog box shows the default driver memory setting while the **Allocated** value displays the amount of contiguous memory that has been allocated successfully. The default values will generally satisfy the needs of most applications.

The **Sapera buffer** values determine the total amount of contiguous memory reserved at boot time for the allocation of dynamic resources used for host frame buffer management, such as DMA descriptor tables as well as other kernel needs. Adjust this value higher if your application generates any out-of-memory error while allocating host frame buffers. You can approximate the amount of contiguous memory required as follows:

- Calculate the total amount of host memory used for frame buffers
  (number of frame buffers • number of pixels per line • number of lines • (2 (if buffer is 10 or 12 bits)).
- Provide 1MB for every 256MB of host frame buffer memory required.
- Add an additional 1MB if the frame buffers have a short line length, for example, 1k or less (increased number of individual frame buffers requires more resources).

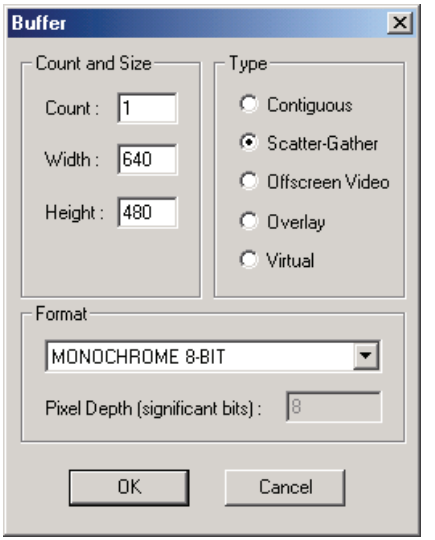
Add an additional 2MB for various static and dynamic

- Sapera resources.
- Test for any memory error when allocating host buffers. Simply use the “General Options” in the Grab Demo Main Window (see page 113) menu of the Sapera Grab Demo program (see "Using the Grab Demo" on page 113) to allocate the number of host buffers required for your acquisition source. Feel free to test the maximum host buffer limit possible in your host system – Grab Demo will not crash when the requested number of host frame buffers cannot be allocated.

Host Computer Frame Buffer Memory Limitations

When planning a Sapera application and the host frame buffers used, as well as other Sapera memory resources, do not forget the needs of the Windows operating system memory. Window® XP, as an example, should always have a minimum of 128MB for its own use.

A Sapera application using *scatter-gather buffers* could consume most of the remaining system memory. When using frame buffers allocated as a *single contiguous memory block*, typical limitations are one third of the total system memory with a maximum limit of approximately 100MB. Click on **Buffer** under Grab Demo Main Window (see page 113) to select from a list of host buffer memory allocation types.



Contiguous Memory for Sapera Messaging

The current value for **Sapera messaging** determines the total amount of contiguous memory reserved at boot time for message allocation. This memory space is used to store arguments when a Sapera function is called. Increase this value if you are using functions with large arguments, such as arrays, and when experiencing any memory errors.

IFC Development Software Overview

IFC-SDK™

The IFC (Imaging Foundation Classes) library offers a C++ Application Program Interface (API) intended for use with the DALSA PC2-Vision board (requires IFC version 5.8 or higher).

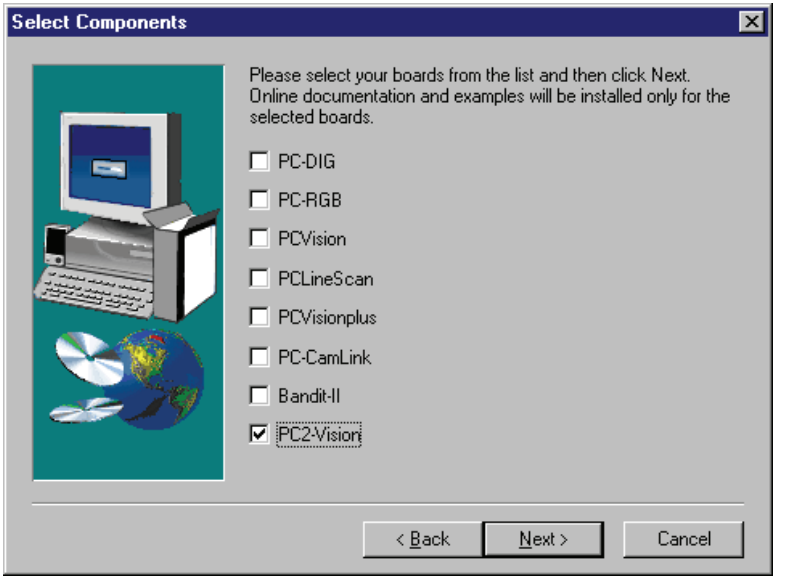
IFC is packaged within the "Imaging Studio CD-ROM".

See the *IFC-SDK™ Software Manual* for information concerning IFC.

Information in this manual matches IFC 5.8 service pack 1.

IFC Software Installation

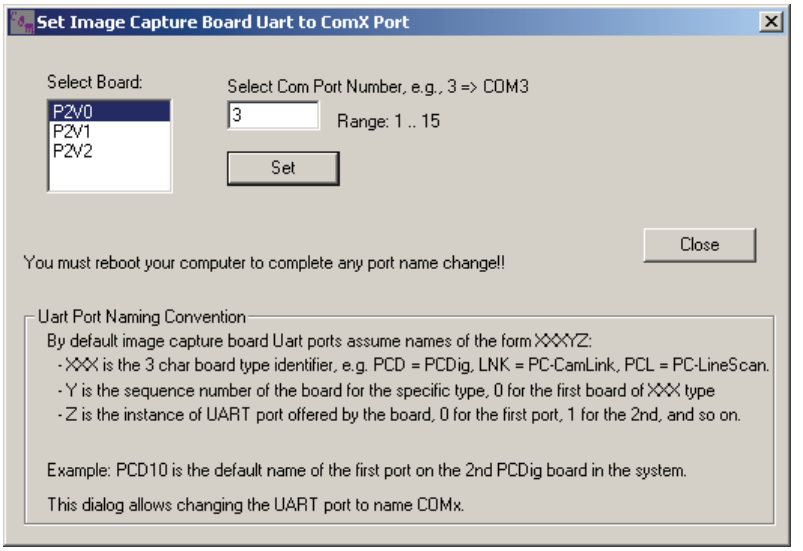
- Make certain that you are logged into your machine with 'administrator' privileges.
- Insert the "Imaging Studio CD-ROM".
- Click on Install Software after auto-start initiates.
- Select OS system and software to install in the pull-down menu and click Start Install.
- Make certain that all window applications are closed before clicking Next in the "Welcome" window.
- Click Yes after reading the Software License Agreement.
- Enter your name and company in the "User Information" window and click Next.
- Click Next in the "Choose Destination Location" window if you want the software to install in the default folder. Click Browse to select another folder if desired.
- If **Browse** is selected, click **OK** in the "Choose Folder" window after path, directory, and driver selections are made.
- The "Setup" window opens and asks if it can create the destination folder displayed. Click **Yes**.
- The "Choose Destination Location" window reopens. Click **Next**.
- The "Setup Type" window is displayed. It is recommended to select the *typical* installation. Click Next.



- The "Select Components" window is displayed (see above screen shot). Check *PC2-Vision* and click Next. Note that only the support, configuration files and examples for the board(s) chosen get copied to your hard drive.
- The "Select Components" window is displayed a second time with a default list of cameras. Select a camera from the default list or select None. If None is selected, a camera file is not installed; however, you can use the Camera Configurator® at anytime after installation to install a camera file.
- After clicking Next in the "Select Program Folder" window, the software and files install unto your hard drive.
- A window appears asking if you want Acrobat Reader installed to view and print installed manuals. Click Yes if you do not already have Acrobat Reader installed on your system.
- Click Yes or No after a window appears asking to view readme files.
- The "Service Pack Update Check" window is displayed. This allows you to check for an IFC service pack update via the DALSA web site. Note that you need an active Internet connection. Click Yes if you want to check for an update.
- The "Setup Complete" window appears and asks whether you want to restart the computer now or at a later time. Choose desired option and click Finish. Note that the computer must be restarted for drivers to take effect.

Optional COM Port Assignment

The IFC "Set Board COM port" application tool is used to assign the COM port. Run the program from the Windows Start menu: **Start♦Programs♦IFC version 5.8♦Set Board COM port**.



To assign a standard COMx name to PC2-Vision:

- Under "Select Board" choose the PC2-Vision board you want to map (P2V0 is the first PC2-Vision board, P2V1 is the second…).
- Under "Select COM port Number" assign an unused COM port number to the PC2-Vision board and click **Set**.
- Click **Close**.
- Reboot PC for the new settings to take effect.

Theory of Operation

PC2-Vision Flow Diagram

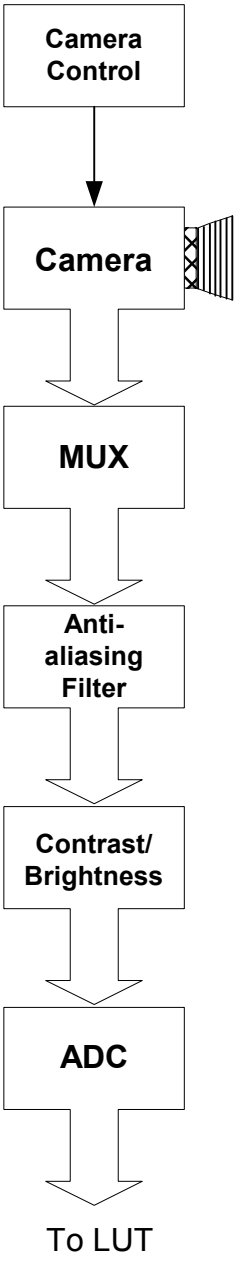
The following three diagrams represent the sequence and components in which the data acquired from the camera is piloted and processed through the PC2-Vision. The process is broken down into three stages:

- Analog Stage
- Pre-Memory Operations
- Post-Memory Operations

Note: the diagrams are broken into three stages for user clarity. In reality the data flow in 'real-world' operation is a continuous stream in which all three stages act as a single process.

The remainder of this chapter will detail features associated with this flow diagram in order of appearance from the camera control to the PCI or PCI Express controller.

Analog Stage



- Seperate HS, VS, FR and WEN to each camera
- Serial Port

- 6 monochrome or 2 RGB or 2 dual-channel cameras

- 3 x 2:1 MUX acquires up to 3 synchronized channels (genlock camera or RGB)

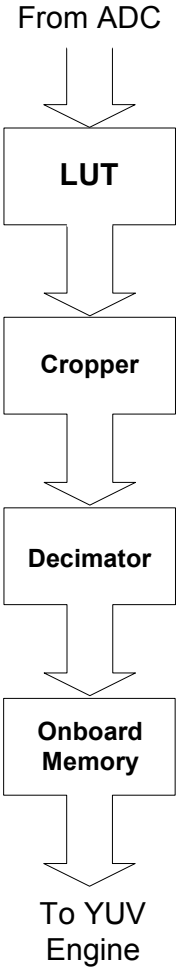
- 6MHz or 12MHz anti-aliasing filter (can be bypassed). SW controlled

- Contrast and brightness control (gain and offset) to use full dynamic range before digital conversion

- High accuracy 40MHz triple channel 8-bit ADC

Figure 3: Analog Stage of Flow Diagram

Pre-Memory Operations



- 8-bit LUT, 1 per camera (total of 6 LUTs onboard)
- Create region of interest
- Image decimation by 2, 4, or 8 horizontally and vertically (pixel dropping)
- 8MB
- Maximum frame size of 2k x 2k mono, or 1k x 1k RGB. Ensures 2 frames in onboard memory for double buffering
- All cameras must have the same frame size when starting an acquisition

Figure 4: Pre-Memory Stage of Flow Diagram

Post-Memory Operations

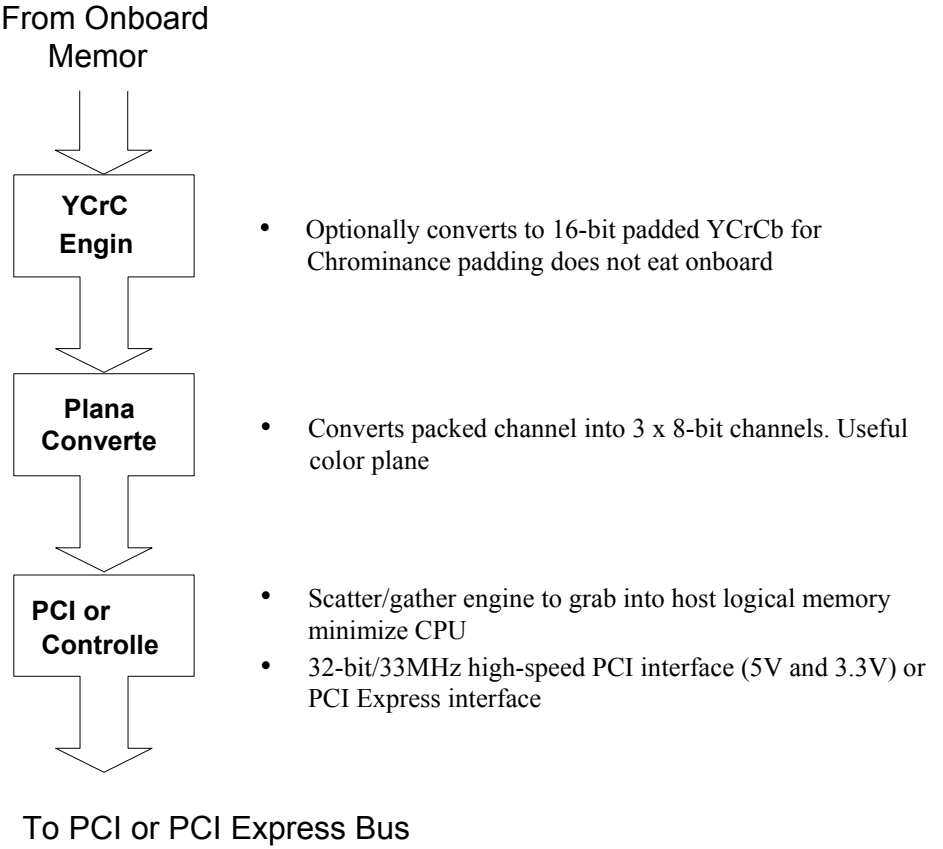


Figure 5: Post-Memory Stage of Flow Diagram

Camera Control and Synchronization

Source of Synchronization

PC2-Vision offers a selection of synchronization sources allowing it to interface with various cameras. All six cameras have their own HS, VS, frame reset and WEN signal. The Acquisition and Control Unit (ACU) is the main controller responsible for supervising the acquisition process. It manages all the signals coming from the cameras and recovers the timing information to accurately digitize the video signal into pixels.

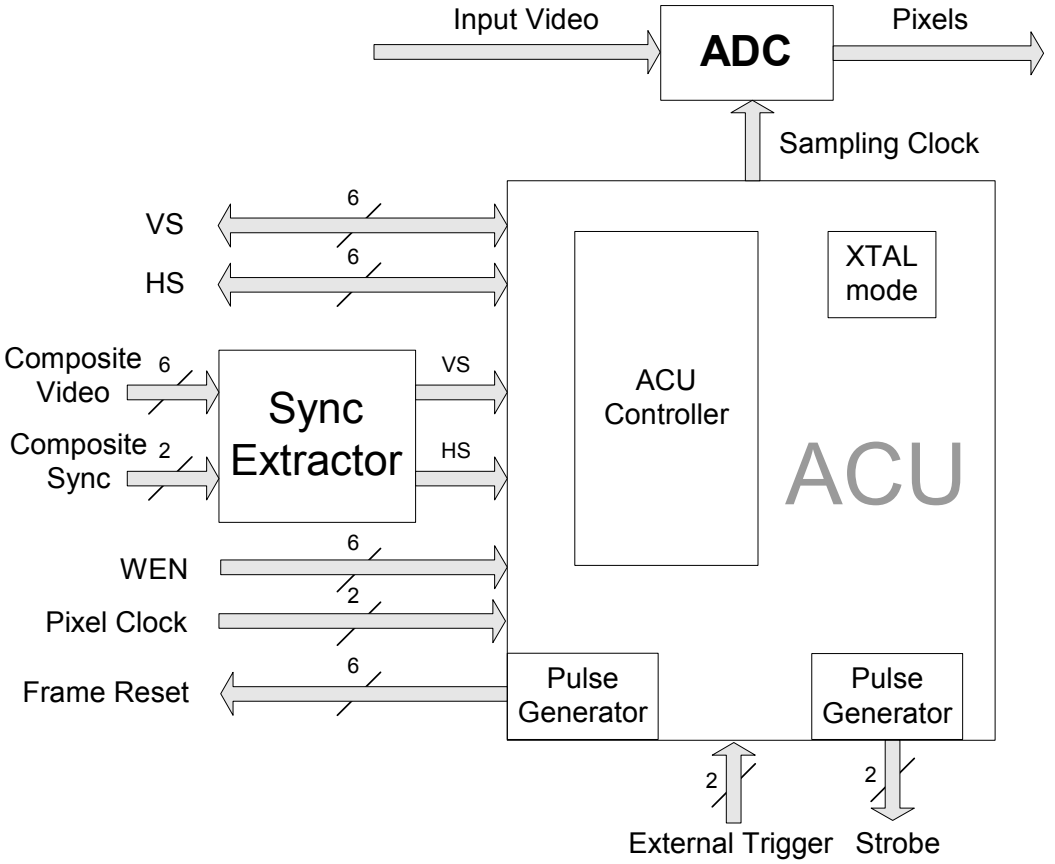


Figure 6: Synchronization Block Diagram

Sync on Composite Video

Vertical Sync (VS) and horizontal sync (HS) signals are extracted from the composite video output signal by the Sync Extractor. The PLL receives the stripped horizontal sync and outputs a pixel clock which is line-locked to the incoming video and is used to digitize video and generate frame timing. The PLL is programmed based on the timing requirements of the incoming video. The ADC uses the PLL generated pixel clock to digitize the video input.

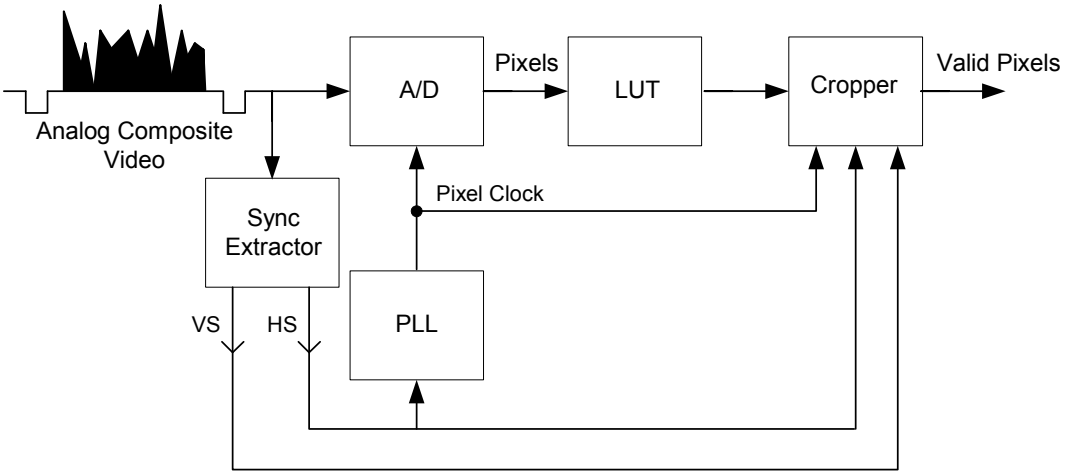


Figure 7: Composite Video

Synchronization on composite video is commonly used for standard RS-170 and CCIR cameras as well as for many non-standard cameras. Video input pins are 75Ω terminated.

Sapera parameters for Sync on Composite Video:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_COMP_VIDEO

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Sync on Composite Video:

P2V_SYNC_SOURCE = P2V_SYNC_COMPOSITE_VIDEO

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Sync on R, G, or B

Sync on R, G, or B behaves like sync on composite video with the exception that only one color channel is used to synchronize the three-color inputs. Timing information is extracted from the selected composite video signal and is common to all three inputs. Asynchronous inputs are not supported by the PC2-Vision. The timing and synchronization settings apply to all three channels.

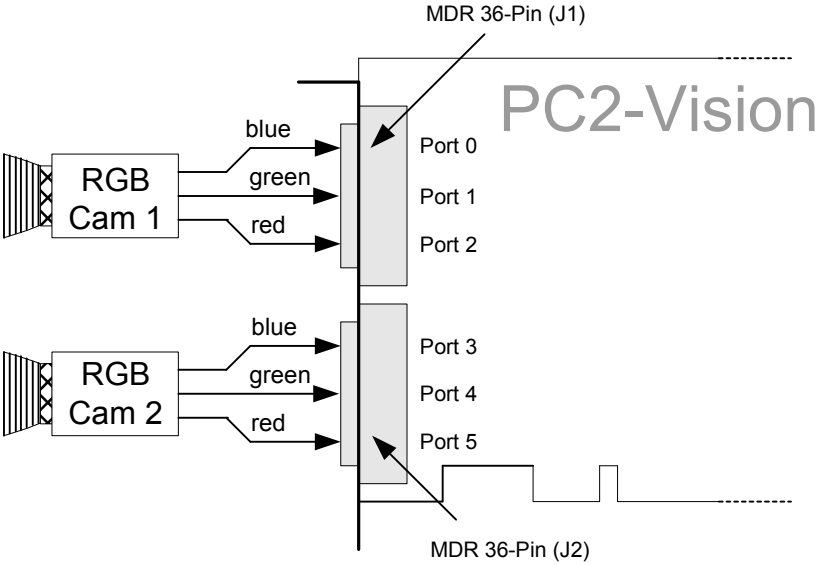


Figure 8: Sync on R, G, or B

Note: that for an RGB camera, the green channel is used as the timing reference if sync on composite video is selected.

Note: Dual-channel cameras are not currently supported with the PC2-Vision Sapera driver.

Sapera parameters for Sync on R, G or B:

CORACQ_PRM_VIDEO = CORACQ_VAL_VIDEO_RGB

CORACQ_PRM_SYNC = { CORACQ_VAL_SYNC_RED, CORACQ_VAL_SYNC_GREEN, CORACQ_VAL_SYNC_BLUE}

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

Dual-channel cameras must use the blue and green channels paired together. PC2-Vision supports the following dual-channel cameras under IFC:

- Channel 1 is always even field (blue channel, port 0 or 3)
- Channel 2 is always odd field (green channel, port 1 or 4)

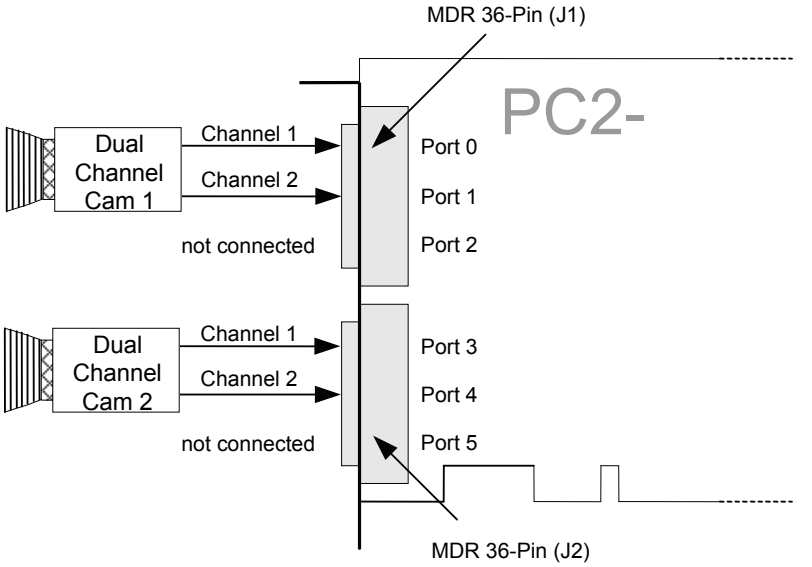


Figure 9: Dual Channel Cameras for IFC

IFC parameters for Sync on R, G or B:

P2V_SYNC_SOURCE = {P2V_SYNC_RED, P2V_SYNC_GREEN, P2V_SYNC_BLUE}

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

P_PIXEL_COLOR = IFC_RGB

P2V_MULTITAP_MODE = {P2V_SINGLE_TAP, P2V_2TAP_ILACE_FIXED}

Sync on Composite Sync

The VS and HS signals are extracted from the composite sync camera output signal and fed into the Sync Extractor to recover horizontal and vertical timing. This information is then used by the PLL to generate the Pixel Clock used by ADC. PC2-Vision supports an analog composite sync signal with a maximal voltage range from 0V to 5V.

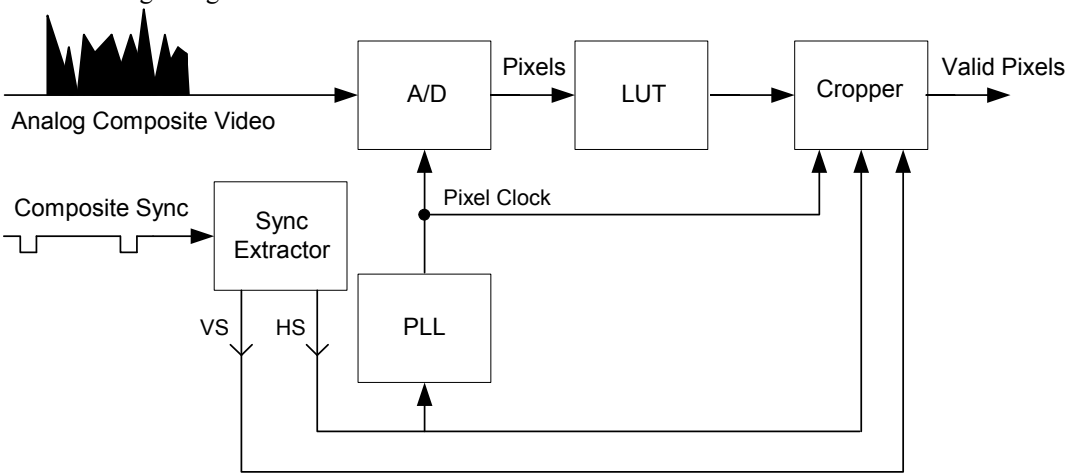


Figure 10: Composite Sync

This mode is generally used for RGB cameras. As such, two composite sync inputs are available on PC2-Vision: one on the first MDR-36 connector (J1) and one on the second (J2).

Sapera parameters for Sync on Composite Sync:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_COMP_SYNC

CORACQ_PRM_VIDEO = CORACQ_VAL_VIDEO_RGB

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Sync on Composite Sync:

P2V_SYNC_SOURCE = P2V_SYNC_COMPOSITE_SYNC

P_PIXEL_COLOR = IFC_RGB

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Sync on Separate Sync

In this mode the VS and HS signals are each input to the PC2-Vision. The Sync Extractor is bypassed. The PLL compares the separate horizontal sync input to the internal feedback and generates the PLL clock. The ADC uses the PLL clock to digitize the video input. The polarity of the sync inputs is programmable, allowing positive or negative polarity inputs (active-high or active-low signals). The incoming signals must be referenced to ground.

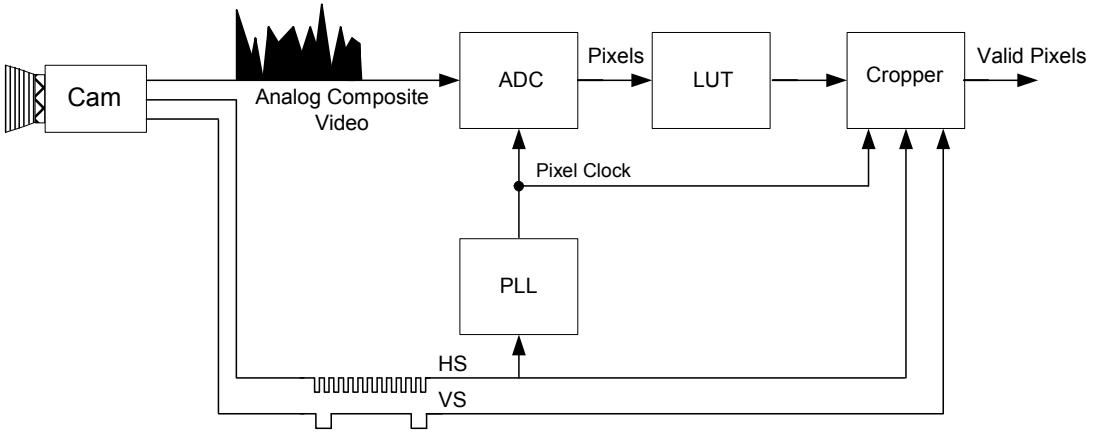


Figure 11: Separate Sync

Each camera has its own VS and HS pin. They are TTL level and are typically implemented using a LVT245 device.

Sapera parameters for Sync on Separate Sync:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_SEP_SYNC

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Sync on Separate Sync:

P2V_SYNC_SOURCE = P2V_SYNC_SEPARATE_SYNC

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Internal Sync

In Internal Sync (XTAL) mode, a clock generator is programmed to generate the desired pixel clock and time base signals. The Clock Generator produces separate horizontal and vertical sync signals that match the desired video format. These signals are then output to the camera. The frequency synthesizer can be programmed to generate any clock frequency up to 40MHz with less than 1ns jitter. In XTAL mode, the Clock Generator can be programmed to standard and non-standard camera timing.

The horizontal and vertical timing created by the Clock Generator is output to the camera as HD/VD signals: called Master Mode. It is also possible to deactivate the VD output so it does not reach the camera. In Master Mode, the PC2-Vision generates VD and/or HD to the camera if the source of synchronization used for digitization is Internal Sync.

Note that a PC2-Vision in Master Mode (that is, driving VD/HD) is independent from the selected source of synchronization. It is therefore possible for PC2-Vision to drive VD/HD to the camera, but still synchronize to the VS/HS present in the composite video signal.

PC2-Vision allows the same VD/HD to be sent to all six cameras simultaneously. This is useful to genlocked cameras together.

HD is used on some cameras to minimize jitter with respect to the frame reset signal. Note that for this to work successfully the HD edge must be aligned with frame reset (refer to camera user's manual). One HD signal is output per active camera.

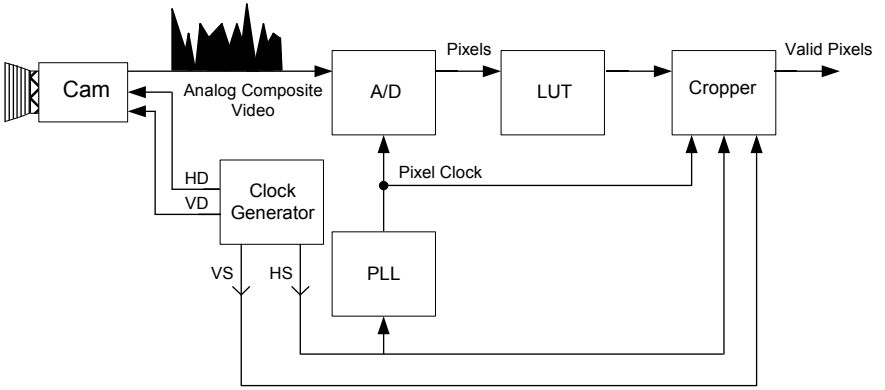


Figure 12: Internal Sync

When using Internal Sync, the horizontal reference for acquisition is HD. This is equivalent to a horizontal front porch of 0 pixels. The horizontal reference is used as a time reference to configure the clamping pulse delay and duration parameters.

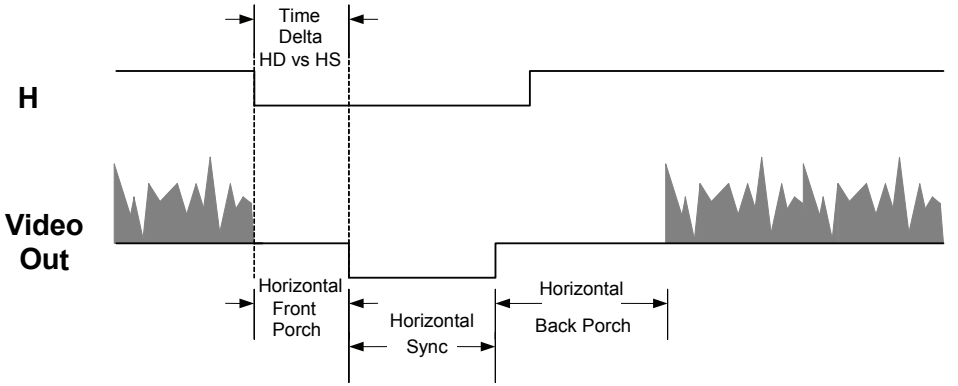


Figure 13: HD relation to HS

Each camera has its own VS and HS pin. They are 3.3V low-voltage TTL level and are typically implemented using a LVT245 device with the following electrical characteristics.

Electrical parameters	Description	Value
$V_{OH\ typ}$	Typical high-level output voltage	3.1V @ -100µA
$I_{OH\ max}$	Maximum high-level output current	-32mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	64mA (sinking)

Sapera parameters for Sync on Internal Sync:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_INT_SYNC

CORACQ_PRM_MASTER_MODE =
CORACQ_VAL_MASTER_MODE_HSYNC_VSYNC

CORACQ_PRM_MASTER_MODE_HSYNC_POLARITY = {
CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_MASTER_MODE_VSYNC_POLARITY = {
CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' and the 'Advanced Control Parameters" tabs.

IFC parameters for Sync on Internal Sync:

P2V_SYNC_SOURCE = P2V_SYNC_INTERNAL_SYNC

P2V_MASTER_HSYNC = IFC_ENABLE

P_HSYNC_FREQ: Horizontal sync pulse frequency

P_HSYNC_WIDTH: Horizontal sync pulse width

P_HSYNC_POLARITY: Horizontal sync pulse polarity

P2V_VS_PULSE_ENABLE = IFC_VSYNC_LINE_WIDTH

P_VSYNC_FREQ: Vertical sync pulse frequency

P_VSYNC_WIDTH: Vertical sync pulse width

P_VSYNC_POLARITY: Vertical sync pulse width

P2V_VSYNC_OUT_ENABLE = {IFC_DISABLE, IFC_ENABLE}

P2V_SYNC_OUT_ALL_CONN = {IFC_DISABLE, IFC_ENABLE}

Note: With Asynchronous Reset mode and synchronization on Internal Sync, use P2V_VS_PULSE_ENABLE = IFC_VSYNC_DISABLE in order for the frame reset and internal VS pulse to be synchronized together. Otherwise, your image will shift vertically while grabbing since the Master Mode VS is not synchronized to frame reset.

WEN

Some cameras indicate when valid data is being delivered by generating WEN, or Write ENable. The function of WEN is similar to a vertical sync pulse. When enabled, the PC2-Vision uses WEN as the vertical timing reference instead of VS. Some cameras generate WEN, but with no VS pulse embedded inside the composite video signal.

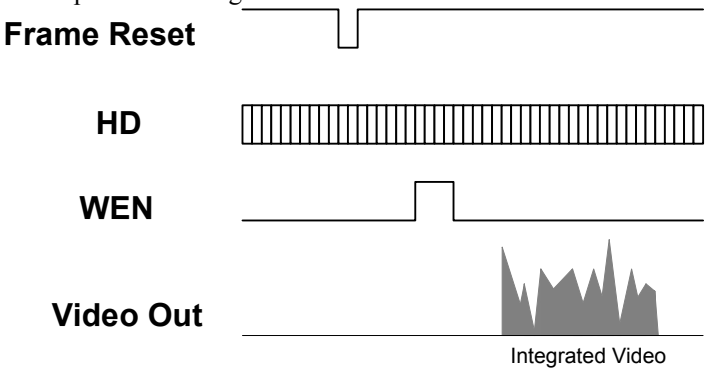


Figure 14: WEN

One WEN signal is available per connected camera. WEN has programmable polarity; it can be selected to be active high or active low. WEN input signal is TTL level and is typically implemented using a LVT244 device.

Sapera parameters for WEN :

CORACQ_PRM_WEN_ENABLE = {TRUE, FALSE}

CORACQ_PRM_WEN_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_VBACK_INVALID: Number of lines to skip for valid video after WEN pulse

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab.

IFC parameters for WEN :

P_WEN_ENABLE = IFC_ENABLE

P_WEN_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_WEN_VERTICAL_OFFSET: Number line to skip for valid video after WEN pulse

Variable Scan Mode

Variable Scan mode is similar to Separate Sync with the addition of a pixel clock signal. Variable Scan mode allows the camera to completely generate the timing information (HS, VS, and pixel clock). The incoming signals must be referenced to ground.

The Pixel Clock (rising edge TTL) is used by the ADC to sample the video signal. One pixel clock signal is available per MDR 36-pin connector. The minimum frequency rate is 7MHz and the maximum is 40MHz. Pixel clock signal supports a TTL voltage range from 0 to 5V.

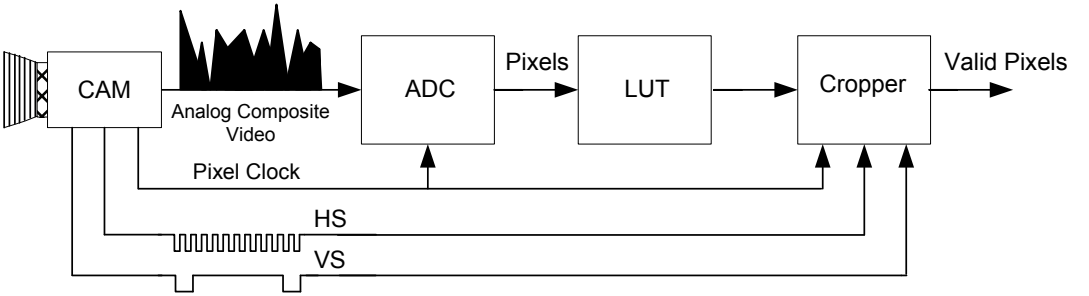


Figure 15: Variable Scan Mode

Sapera parameters for Variable Scan Mode:

CORACQ_PRM_SYNC = CORACQ_VAL_SYNC_SEP_SYNC

CORACQ_PRM_PIXEL_CLK_SRC = CORACQ_VAL_PIXEL_CLK_SRC_EXT

CORACQ_PRM_PIXEL_CLK_EXT: External pixel clock frequency in Hz

CORACQ_PRM_HSYNC: Size of horizontal sync pulse

CORACQ_PRM_HSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_HBACK_PORCH: Size of horizontal back porch

CORACQ_PRM_HACTIVE: Number of valid pixels per line

CORACQ_PRM_HFRONT_PORCH: Size of horizontal front porch

CORACQ_PRM_VSYNC: Size of vertical sync pulse

CORACQ_PRM_VSYNC_POLARITY = {CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_VBACK_PORCH: Size of vertical back porch

CORACQ_PRM_VACTIVE: Number of valid line from camera

CORACQ_PRM_VFRONT_PORCH: Size of vertical front porch

In CamExpert, these parameters are located under the 'Basic Timing Parameters' tab.

IFC parameters for Variable Scan Mode:

P2V_SYNC_SOURCE = P2V_SYNC_SEPARATE_SYNC

P_PIXEL_CLK_SIGNAL_TYPE = P2V_PIXEL_CLOCK_EXTERNAL

P_HSYNC_FREQ: Horizontal sync frequency

P_HSYNC_WIDTH: Size of Horizontal sync pulse

P_HSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_HORZ_FRONT_PORCH: Size of horizontal front porch

P2V_HORZ_BACK_PORCH: Size of horizontal back porch

P_VSYNC_FREQ: Vertical sync frequency

P_VSYNC_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_NUM_EQ_PULSES_FPORCH: Size of vertical front porch

P_NUM_EQ_PULSES_BPORCH: Size of vertical back porch

Camera Control

Pulse Generator

PC2-Vision has three independent timers that control pulse generation. This is necessary for camera control. This allows to position pulses precisely (to a resolution of 1µs) relative to the triggering event. This flexibility proves very handy considering the wide range of camera control modes (edge pre-select, pulse width control, E-Donpisha, etc.).

An independent timer is available for each of the following signals:

- VS
- Frame Reset
- Strobe

VS and Frame Reset timers can be combined to generate a double-pulse on the same camera pin. This is required for some camera modes, like long time exposure.

Each timer has the following capabilities:

- Programmable polarity (active high or active low)
- Programmable delay from trigger event (up to 65 seconds)
- Programmable duration (up to 65 seconds)

Timer granularity is 1µs when the delay and duration values are below 65ms. Granularity falls to 1ms for delay or duration above 65ms. Delay and duration always have the same granularity level.

Each timer can be started by any of the following events:

- VS
- External trigger
- Software trigger

VS is the default.

Frame Reset

Frame reset—also known as camera reset or camera trigger—is a signal sent by the PC2-Vision to the camera to trigger an acquisition. One frame reset signal is available per camera. The pulse duration and polarity are programmable. Frame reset can be triggered either by an external trigger signal, a software trigger or a VS. After the trigger is initiated, an internal frame reset counter counts up to 65 seconds. This pulse is normally used to control the exposure of the camera CCD (Edge Pre-Select mode or Pulse Width Control mode). The frame reset output signal is 3.3V low-voltage TTL. It is typically implemented using a LVT244 device with the following electrical characteristics.

Electrical parameters	Description	Value
$V_{OH\ typ}$	Typical high-level output voltage	3.1V @ -100µA
$I_{OH\ max}$	Maximum high-level output current	-32mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	64mA (sinking)

Two parameters control the frame reset pulse. First, the offset indicates the delay from the trigger before asserting frame reset. Then, the size specifies the time the frame reset pulse is asserted. The duration of the pulse controls the exposure period on some cameras.

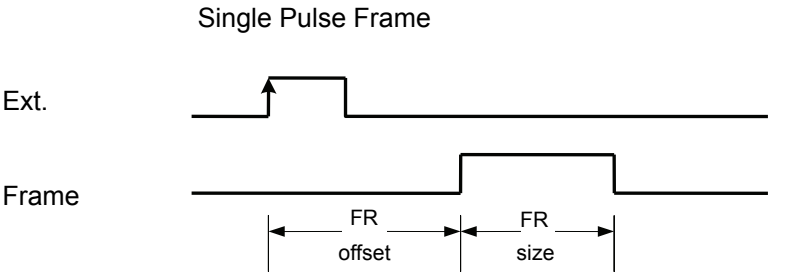


Figure 16: Single pulse frame reset

Warning: Some cameras have frame reset located on pin 9 of the Hirose-12 connector while other cameras have it on pin 11. It is imperative to use the appropriate camera cable that matches the frame reset pinout. Failure to do so could result in board damage.

PC2-Vision provides an additional protection circuit that inhibits an erroneous connection of the frame reset pin, preventing a 12V power level damaging the frame reset output. Nevertheless, it is not recommended to put a 12V level on the frame reset pin.

Sapera parameters for Frame Reset :

Refer to Time Integration method of Sapera documentation.

CORACQ_PRM_TIME_INTEGRATE_METHOD: Method to use for time integration

CORACQ_PRM_TIME_INTEGRATE_PULSE0_DELAY: Pulse offset from trigger event

CORACQ_PRM_TIME_INTEGRATE_PULSE0_DURATION: Size of pulse

CORACQ_PRM_TIME_INTEGRATE_PULSE0_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

Note: Frame reset pulse is always aligned on HS in Sapera.

CamExpert: parameters are located under the 'Advanced Control Parameters' tab.

Under IFC, Frame Reset shares the VS parameters to create a double pulse. A control is offered to add VS to frame reset. In this case, both pulses will be sent to the frame reset pin. Then, it is only a matter of providing the appropriate offset and size for Frame Reset and VS. The distance between the first and second pulse controls the exposure period on some cameras.

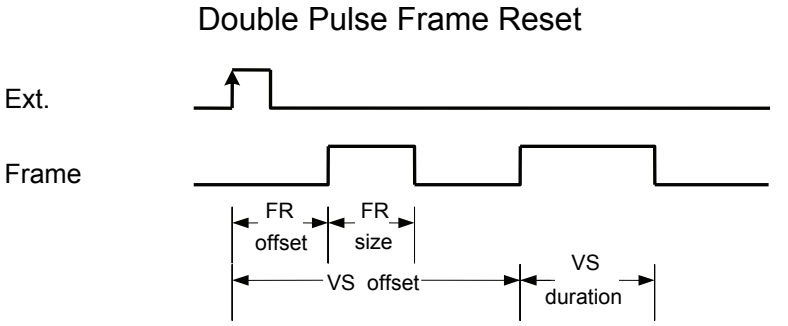


Figure 17: Double pulse frame reset for IFC

IFC parameters for Frame Reset :

P_FRAME_RESET_MODE = IFC_ENABLE

P_FRAME_RESET_POLARITY = {IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P_FRAME_RESET_OFFSET: Pulse offset from trigger event

P_FRAME_RESET_SIZE: Size of pulse

P2V_ADD_FRAME_RESET_TO_VSYNC = {IFC_DISABLE IFC_ENABLE}

P_FRAME_RESET_ALIGN_ON_HS = {IFC_DISABLE, IFC_ENABLE}

VSync

One VS signal is output per active camera. This feature is used on some cameras to control the exposure rate when in Master Mode (XTAL). The VS can generate up to two pulses, each with a different duration up to 65 seconds. VSync output signal is 3.3V low-voltage TTL level. It is typically implemented using a LVT245 device.

Two parameters control the VS pulse. First, the offset indicates the delay from the trigger before asserting VS. Then, the duration specifies the time the VS pulse is asserted.

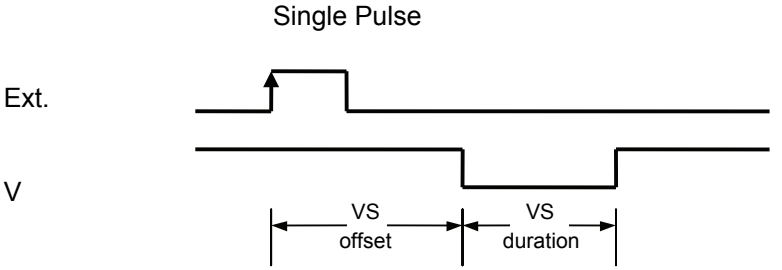


Figure 18: Single pulse VS

Sapera parameters for VSync :

Refer to Time Integration method of Sapera documentation

CORACQ_CAP_TIME_INTEGRATE_METHOD: Method to use for time integration

CORACQ_PRM_TIME_INTEGRATE_PULSE_DELAY: Pulse offset from trigger event

CORACQ_PRM_TIME_INTEGRATE_PULSE_DURATION: Size of pulse

CORACQ_PRM_TIME_INTEGRATE_PULSE_POLARITY = { CORACQ_VAL_ACTIVE_LOW, CORACQ_VAL_ACTIVE_HIGH}

Note: VSync pulse is always aligned on HS in Sapera.

CamExpert: parameters are located under the 'Advanced Control Parameters' tab.

Under IFC, VS shares the frame reset parameters to create a double pulse. A control is offered to add Frame Reset to VS. In this case, both pulses will be sent to the VS pin. Then, it is only a matter of providing the appropriate offset and duration for VS and Frame Reset.

Figure 19: Double pulse VS for IFC

IFC parameters for VSync :

P2V_VS_PULSE_ENABLE = P2V_VSYNC_TIME_WIDTH

P_VSYNC_FREQ: Frequency of VSync pulse

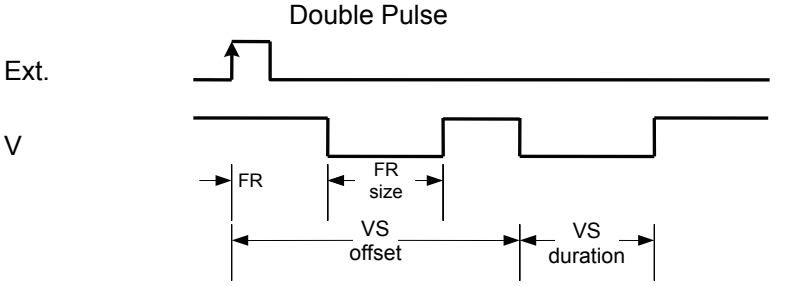
P_VSYNC_WIDTH: Width of VSync pulse

P_VSYNC_POLARITY = { IFC_ACTIVE_LOW, IFC_ACTIVE_HIGH}

P2V_ADD_VSYNC_TO_FRAME_RESET = {IFC_DISABLE, IFC_ENABLE}

P2V_VSYNC_ALIGN_ON_HS = {IFC_DISABLE, IFC_ENABLE}

P2V_VSYNC_OUT_ENABLE = {IFC_DISABLE, IFC_ENABLE}



External Trigger and Strobe

External Trigger

External Trigger allows image acquisition to be synchronized to external events. When acquiring an image in External Trigger mode, the acquisition will not start until the PC2-Vision receives a trigger signal. Acquisition begins with the next valid frame after the trigger.

One external trigger signal is available per MDR 36-pin connector. The external trigger is protected by an opto-coupler. The external trigger can be driven by any voltage source from 3.3V low-voltage TTL up to 24V, as long as it can provide at least 2mA.

The incoming trigger pulse is "debounced" to ensure that no glitch would be detected as a valid trigger pulse. This debouncer can be programmed from 0μs to 255μs. Any pulse smaller than the programmed value will be blocked and therefore not be seen by the acquisition circuitry.

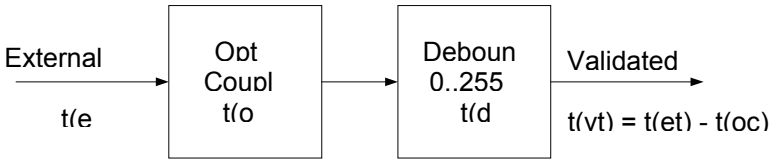


Figure 20: External Trigger

Let t(et) = time of external trigger in μs
t(vt) = time of validated trigger in μs
t(oc) = time opto-coupler takes to change state
t(d) = debouncing duration from 0 to 255μs

For an active high external trigger, t(oc) = 10μs:
t(vt) = t(et) – 10μs – t(d)

For an active low external trigger, t(oc) = 50μs:
t(vt) = t(et) – 50μs – t(d)

Note: DALSA recommends using a rising edge external trigger in order to minimize the time it takes for the opto-coupler to change state. That is, the opto-coupler response time is 10μs for rising edge compared to 50μs for falling edge. DALSA also recommends putting a debouncing duration of at least 1μs to guaranty that opto-coupler transitions cannot be falsely detected by the TTL logic.

If t(vt)> 0, then a valid trigger is detected and acquisition is fired. Therefore, the external pulse with rising edge polarity must be at least 10μs (if debouncer is set to 0) in order to be acknowledged. Any pulse larger than 265μs is always considered valid.

It is possible to emulate an external trigger using the software trigger. The latter is generated by a function call from the application.

External trigger is supported using two pins: Ext_Trigger- and Ext_Trigger+. RS-422 level can be directly connected to those pins. When using TTL level, connect the Ext_Trigger- to ground and drive Ext_Trigger+ with the TTL trigger.

The PC2-Vision external trigger interfaces to the external world through the use of an opto-coupled device. Formed by an LED emitter combined with a photodetector in close proximity, an opto-coupler (or opto-isolator) connects the PC2-Vision external trigger and the user circuit together while using separate grounds. This “galvanic isolation” approach prevents ground loops and protects both circuits. A serial resistor of 650Ω is connected in serial to the opto-coupler to limit the current.

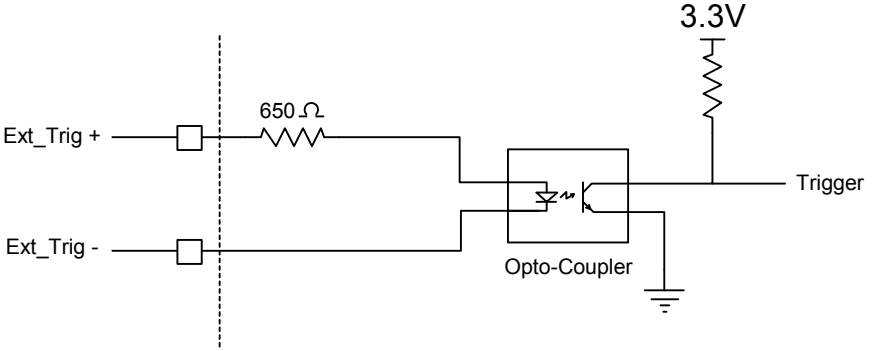


Figure 21: Opto-coupler

When current flows inside the LED, the emitted light acts as a base current for the transistor. Depending on the amount of light being emitted, the transistor can be turned ON just like a switch. Data in the form of a voltage is transmitted on one side to the other like a transistor being ON or OFF. The opto-coupler input is an inverting circuit, but the PC2-Vision software compensates for this when specifying the polarity.

The surrounding circuit that converts the voltage to flow as a current into the LED is therefore crucial to the good performance of the opto-coupler. The emitted light will not turn the transistor ON if the current flowing through the LED is too small. The opto-coupler on the PC2-Vision is typically a Fairchild HMHA281 with the following characteristics:

Electrical parameters	**Description**	**Value**
$V_{IL\ max}$	Maximum voltage difference to turn OFF	0.8 V
$V_{IH\ min}$	Minimum voltage difference to turn ON	2 V
$I_{I\ min}$	Minimum input current to turn ON	2 mA
$I_{I\ max}$	Maximum input current to turn ON	50 mA
$t_{I\ min}$	Minimum input pulse width to turn ON	10 us
$V_{f\ max}$	Maximum forward voltage	24 V
$V_{r\ max}$	Maximum reverse voltage	-25 V

Note: TTL signals are approximately 0 and 3.3/5V, corresponding to logical 0 and 1, respectively. A standard TTL output can sink 16mA and could be used as a sink to drive an opto-coupled input. That is, +5V is connected to Ext_Trig+ and the sink trigger source is connected to Ext_Trig-. This will normally require the application to invert the polarity of the trigger in the camera configuration file.

Sapera parameters for External Trigger:

CORACQ_PRM_EXT_TRIGGER_ENABLE = CORACQ_VAL_EXT_TRIGGER_ON

CORACQ_PRM_EXT_TRIGGER_SOURCE = {0: Same connector as video source, 1: first MDR-36, 2: second MDR-36}

CORACQ_PRM_EXT_TRIGGER_DETECTION = {CORACQ_VAL_RISING_EDGE, CORACQ_VAL_FALLING_EDGE, CORACQ_VAL_ACTIVE_LOW. CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_EXT_TRIGGER_DURATION: Debouncing duration

CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT: Number of frame to acquire per trigger

Note: CORACQ_PRM_EXT_TRIGGER_LEVEL always represents the opto-coupler trigger input independent of its actual value (CORACQ_VAL_LEVEL_TTL or CORACQ_VAL_LEVEL_422). This means this parameter "does not matter" for the PC2-Vision driver.

In CamExpert, these parameters are located under the 'External Trigger Parameters' tab.

IFC parameters for External Trigger:

P_TRIGGER_ENABLE = IFC_ENABLE

P_TRIGGER_SRC = {IFC_SOFT_TRIG, IFC_EXT0_TRIG, IFC_EXT1_TRIG, IFC_EXT_AUTO_TRIG}

P_GEN_SW_TRIGGER = {0, 1}

P_TRIGGER_POLARITY = {IFC_FALLING_EDGE, IFC_RISING_EDGE}

P_FRAMES_PER_TRIGGER: Number of frames to acquire per trigger

P_TRIGGER_DEBOUNCE: Debouncing duration

P2V_VSYNC_WAIT_COUNT: Number of VS to count before acquiring after a trigger

Strobe

One strobe signal is output per MDR 36-pin connector. The pulse duration and polarity are programmable (up to 65 seconds).

The strobe signal is achieved using a LVT244 driver with the following electrical characteristics:

Electrical parameters	Description	Value
$V_{OH\ typ}$	Typical high-level output voltage	3.1V @ -100µA
$I_{OH\ max}$	Maximum high-level output current	-32mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	64mA (sinking)

Sapera parameters for Strobe :

Refer to Strobe Method in Sapera documentation

CORACQ_PRM_STROBE_ENABLE = TRUE

CORACQ_PRM_STROBE_LEVEL = CORACQ_VAL_LEVEL_TTL

CORACQ_PRM_STROBE_METHOD = {CORACQ_VAL_STROBE_METHOD_1, CORACQ_VAL_STROBE_METHOD_2}

CORACQ_PRM_STROBE_POLARITY = {CORACQ_VAL_ACTIVE_LOW

, CORACQ_VAL_ACTIVE_HIGH}

CORACQ_PRM_STROBE_DELAY: Pulse offset from trigger event

CORACQ_PRM_STROBE_DELAY_2: Duration of exclusion region

CORACQ_PRM_STROBE_DURATION: Pulse duration

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab.

Under IFC, PC2-Vision offers two types of strobes: Fast Strobe (equivalent to Strobe Method 1 of Sapera) and Slow Strobe. Fast strobe occurs immediately after the trigger. See below for diagram. The first falling edge of the trigger immediately generates a strobe pulse. The strobe pulse duration is programmable. This mode is often used with asynchronous reset cameras.

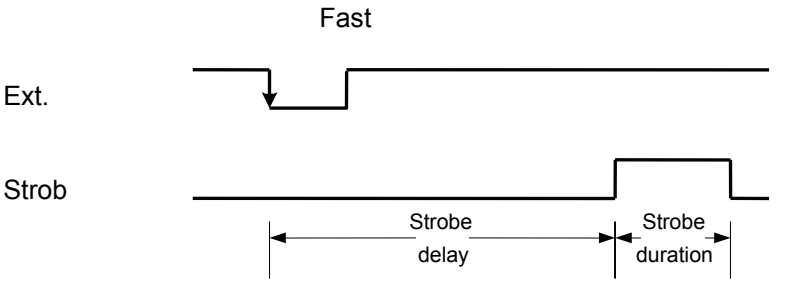


Figure 22: IFC Fast Strobe

Note: PC2-Vision does not support an exclusion region in Fast Strobe mode. Strobe delay parameter represents the time from the external trigger to strobe pulse assertion.

In Slow Strobe mode, the strobe pulse occurs after a certain delay following the VS and the trigger, respectively. Strobe duration is programmable. See below for diagram. Basically, the strobe pulse is asserted from the first VS following the trigger. This mode is often used with free-running cameras.

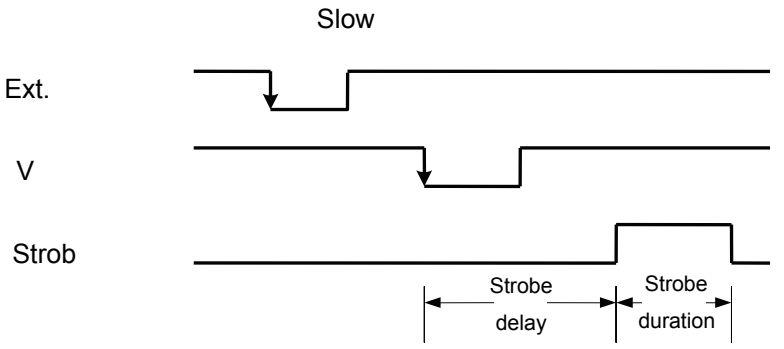


Figure 23: IFC Slow strobe

IFC parameters for Strobe :

P_STROBE_ENABLE = IFC_ENABLE

P_STROBE_MODE = {IFC_FAST_STROBE, IFC_SLOW_STROBE}

P_STROBE_POLARITY = {IFC_ACTIVE_HIGH, IFC_ACTIVE_LOW}

P_STROBE_DELAY: Pulse offset from trigger event

P_STROBE_DURATION: Pulse duration

P_STROBE_ALIGN_ON_HS = {IFC_DISABLE, IFC_ENABLE}

Serial Port

PC2-Vision hosts a serial port UART that can be dynamically mapped to the first or second MDR-36 connector. Therefore, you have two Rx/Tx pairs available from PC2-Vision (even though they both are driven from the same physical UART).

This serial port is intended for camera control.

Default name for this serial port is: **PC2-Vision_*X*_Serial_0**, where *X* represents the PC2-Vision board number, from 1 to 8.

Note: A typical configuration would use 9600 baud♦8-bit♦no parity♦1 stop bit (9600-8-N-1).

Note: After booting your computer, you must run an IFC or a Sapera application, such as the Configurator® or CamExpert, to make the serial port accessible. This is required to initialize resources on the PC2-Vision.

Ports can be used with their default names (for example: PC2-Vision_1_Serial_0) by many camera control applications. Additionally, the serial port can be mapped as a standard Windows COMx port for convenience or compatibility with any communication program (such as HyperTerminal).

Sapera parameters for Serial Port

In Sapera, the serial port is mapped as a regular COM Port. It can be configured through WIN32 API.

Note: In Sapera, the serial port selection always follows the current video source.

IFC parameters for Serial Port

P2V_SELECT_UART_PORT = { P2V_UART_PORT_AUTO, P2V_UART_PORT_CON1, P2V_UART_PORT_CON2}

P_COM_PORT_NAME : String that specifies serial port name

P_COM_PORT_BYTESIZE = {IFC_COM_7BITS, IFC_COM_8BITS}

P_COM_PORT_BAUDRATE = {IFC_BAUD_4800, IFC_BAUD_9600, IFC_BAUD_14400, IFC_BAUD_19200, IFC_BAUD_38400, IFC_BAUD_56000, IFC_BAUD_57600, IFC_BAUD_115200, IFC_BAUD_128000}

P_COM_PORT_PARITY = {IFC_NOPARITY, IFC_ODDPARITY, IFC_EVEN_PARITY}

P_COM_PORT_STOPBITS = {IFC_ONE_STOPBIT}

IFC uses those parameters to communicate with the serial port in the following two cases:

- when the application calls **CICamera::WriteUartCommand()**.

- when IFC uses the rule evaluation from the config file.

Camera Selection (MUX)

The PC2-Vision communicates with the camera through two MDR 36-pin connectors located on the bracket. Each connector can support up to three monochrome, one RGB, or one dual-channel camera(s). Up to six monochrome, two RGB, or two dual-channel cameras, therefore, can be connected to the PC2-Vision at the same time. But only one MDR-36 connector is MUXed to the ADC.

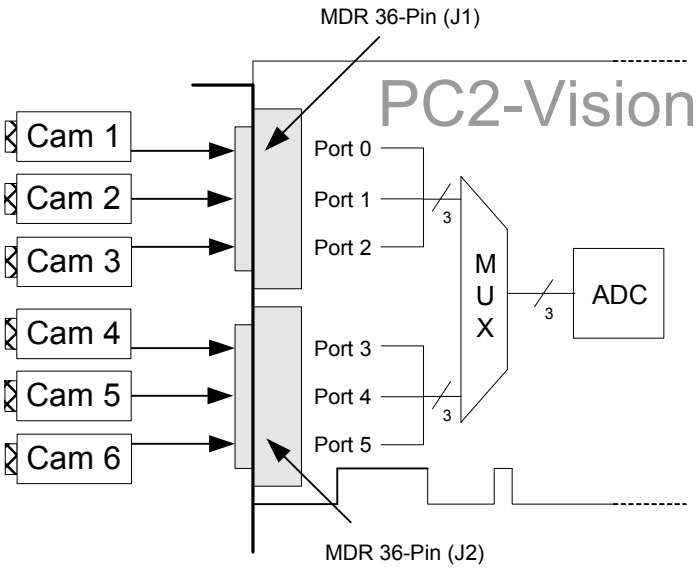


Figure 24: Six monochrome connections

The PC2-Vision can also genlock monochrome cameras attached to the same MDR-36-pin connector and digitize data simultaneously. A 12V power pin (500mA) is supported for each camera (fuse protected). Note that the J6 connector on the PC2-Vision must be connected to a floppy power cable to provide 12V to the cameras. Refer to the "PC2-Vision component view" (on page 72) section for connector locations.

The input is selected by the software control. The timing is common to all three inputs. Independent timing is not available. Asynchronous inputs are not supported by the PC2-Vision. The timing and synchronization settings apply to all three channels synchronously. Multiple monochrome cameras must be externally genlocked or driven by the PC2-Vision timing (see "Internal Sync" on page 32).

PC2-Vision Input	Monochrome Camera	RGB Camera
video 1	CAM 1	CAM1 blue
video 2	CAM 2	CAM1 green
video 3	CAM 3	CAM1 red
video 4	CAM 4	CAM2 blue
video 5	CAM 5	CAM2 green
video 6	CAM 6	CAM2 red

IFC Port	Monochrome Camera	RGB Camera	Dual-Channel Camera
0	CAM 1	CAM1 blue	CAM1 even field
1	CAM 2	CAM1 green	CAM1 odd field
2	CAM 3	CAM1 red	Not used
3	CAM 4	CAM2 blue	CAM2 even field
4	CAM 5	CAM2 green	CAM2 odd field
5	CAM 6	CAM2 red	Not used

For RGB or dual-channel cameras, use IFC port 0 for J1 MDR-36 or port 3 for J2 MDR-36 to control the camera in the application source code.

Anti-aliasing Filter

Following the MUX stage, the video passes through a selectable low-pass filter, optimized for standard video frequencies. The filter values are 6MHz and 12MHz, with the possibility to bypass filters. All three channels are selected together; independent low-pass selection not available. The low-pass filter strips high frequency signal content from the incoming video signal, to avoid sampling aliasing artifacts in the signal. Standard video (RS-170, CCIR) has useful frequency content up to approximately 6MHz. Frequencies above this can be eliminated using the low-pass filters. Sampling rates for standard video are 10MHz (up to 14MHz). If frequencies at or above the sampling rate are present, they represent noise rather than useful video. These frequencies can "alias" into the real video signals causing corruption. The low-pass filters can eliminate any high frequency signal content before digitization.

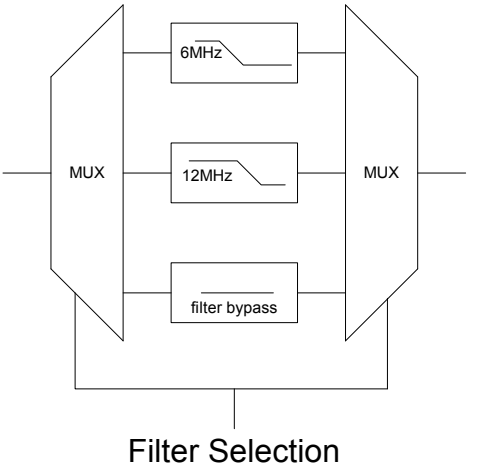


Figure 25: Anti-Aliasing Filter

Sapera parameters for Anti-aliasing Filter:

CORACQ_PRM_FIX_FILTER_ENABLE = {TRUE, FALSE}

CORACQ_PRM_FIX_FILTER_SELECTOR = {0 for 6 MHz, 1 for 12 MHz}

Note: Bypass filter is selected when CORACQ_PRM_FIX_FILTER_ENABLE = FALSE.

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab under the 'Analog Signal Conditioning' entry.

IFC parameters for Anti-aliasing Filter:

P2V_LOW_PASS_FILTER = { P2V_LPF_6_5_MHZ, P2V_LPF_12_MHZ, P2V_LPF_BYPASS}

Contrast and Brightness Adjustment

Contrast and Brightness are controlled through the input gain of the ADC; the PC2-Vision was calibrated during the manufacturing process to support this feature.

Brightness controls the offset of the digitization line while contrast controls its gain (the slope of the line). See below for diagram. The vertical axis represents the voltage level of the incoming video signal (black level is 53mV, white level is 714mV in NTSC) while the horizontal axis shows the resulting pixel value. For instance, using default brightness and contrast, an incoming video signal of 350mV gets digitized into a value of 115. By increasing the brightness, the digitization line gets shifted down, which creates a brighter image (same input voltage leads to a higher pixel value). Decreasing brightness leads to a darker image. Note that changing the brightness only affects the offset of the digitization line, not its slope. This latter attribute is controlled through contrast. By increasing contrast, the slope of the digitization line is decreased, which lowers the voltage difference between two consecutive pixel values.

Default values of brightness and contrast use the full resolution of the ADC for a standard RS-170 source.

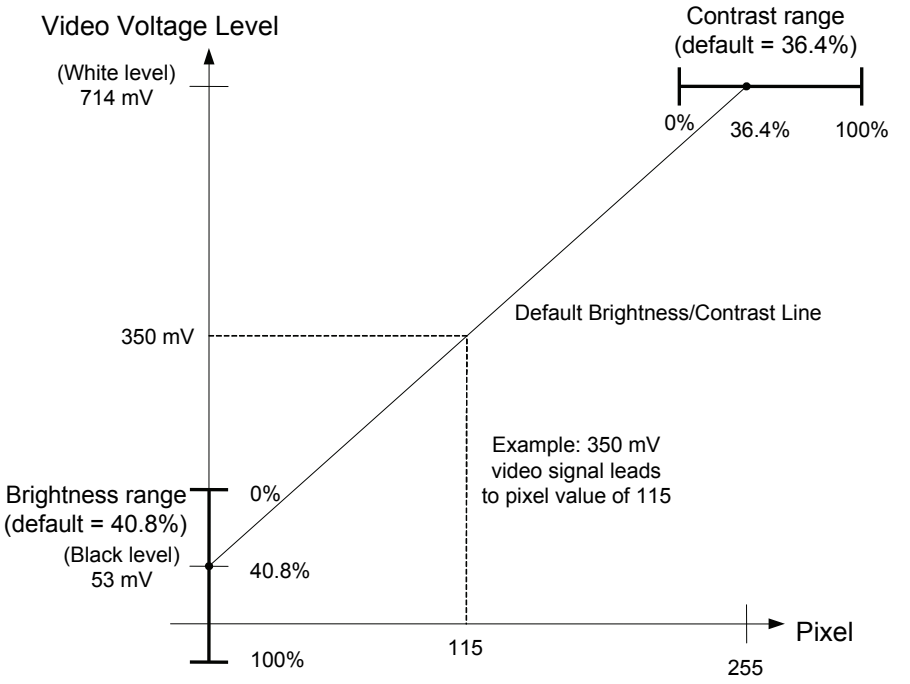


Figure 26: Video voltage level

Sapera parameters for Contrast and Brightness :

CORACQ_PRM_CONTRAST: Contrast percentage

CORACQ_PRM_BRIGHTNESS: Brightness percentage

CORACQ_PRM_VIDEO_LEVEL_MIN: Minimum value (in µV) of the video signal

CORACQ_PRM_VIDEO_LEVEL_MAX: Maximum value (in µV) of the video signal

Note: Under Sapera, contrast percentage ranges from 60% to 170% with 100% being the default value. Brightness percentage ranges from –20% to 29% with 0 % being the default value. Typically, you do not need to adjust the default contrast and brightness if the video level min and video level max parameters matches your camera.

In CamExpert, these parameters are located under the 'Advanced Control Parameters' tab under the 'Analog Signal Conditioning' entry.

IFC parameters for Contrast and Brightness :

P_CONTRAST: Contrast percentage

P_BRIGHTNESS: Brightness percentage

Note: Under IFC, contrast percentage and brightness percentage are normalized from 0% to 100%.

AD Converter

The PC2-Vision uses a 40MHz triple ADC (Analog to Digital Converter). The triple ADC outputs three 8-bit unsigned binary values from 0x0 to 0xFF based on: the sampled analog input signal level, the ADC sampling window of each input channel, and by the clamping voltage level (independent for each channel). The Pixel Clock used by the ADC comes from one of three sources: the PLL clock (PLL mode), the Clock Generator (XTAL mode), or the externally input Variable Scan Clock (Vscan mode).

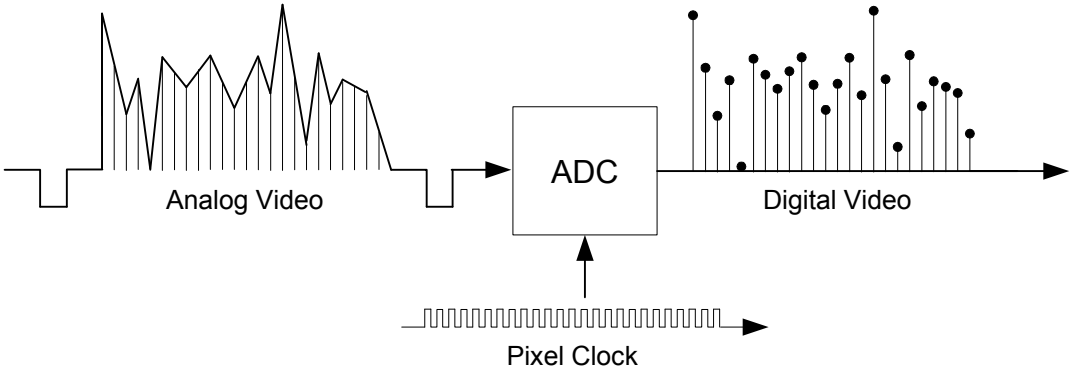


Figure 27: AD Converter

The Pixel Clock is used to sample incoming video signal at the specified frequency. The result is a series of 8-bit digital values representing the analog video signal.

DC Restoration

DC Restoration uses a programmable clamp pulse. It uses the horizontal back porch to establish the reference black video level.

Two parameters are required to indicate the location of the region used as the reference. The *clamp_start* and *clamp_end* parameters refer to the HS edge. The *clamp_width* is the time difference between *clamp_start* and *clamp_end*. See below for diagram.

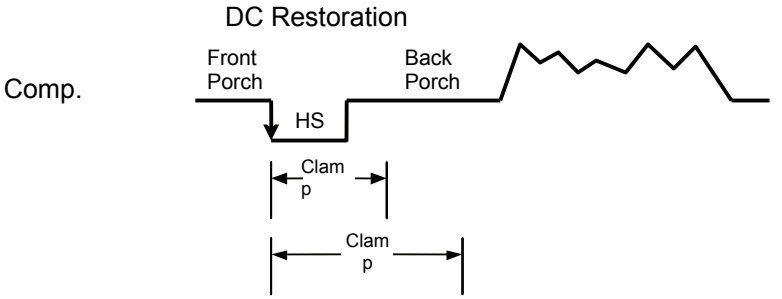


Figure 28: DC restoration

Note: With Internal Sync mode, the horizontal reference is the edge of HD, as shown in "Figure 13: HD relation to HS" (on page 33). With this synchronization scheme, clamp start and clamp end values refer to first edge of HD, not to HS coming from composite video.

Sapera parameters for ADC Converter:

CORACQ_PRM_PIXEL_CLK_INT: Internal pixel clock frequency (in Hz)

CORACQ_PRM_PIXEL_DEPTH = 8

CORACQ_PRM_DC_REST_MODE = { CORACQ_VAL_DC_REST_MODE_AUTO , CORACQ_VAL_DC_REST_MODE_ON, CORACQ_VAL_DC_REST_MODE_OFF}

CORACQ_PRM_DC_REST_START: Start of clamp pulse relative to HS or HD

CORACQ_PRM_DC_REST_WIDTH: Clamp pulse duration

In CamExpert, DC restoration parameters are located under the 'Advanced Control Parameters' tab under the 'Analog Signal Conditioning' entry.

IFC parameters for ADC Converter:

P_PIXEL_CLK_FREQ: Pixel clock frequency

P_PIXEL_SIZE = 8

P_CLAMP_MODE = IFC_ENABLE

P2V_CLAMP_START: Start of clamp pulse relative to HS or HD

P2V_CLAMP_END: End of clamp pulse relative to HS or HD

Lookup Table

A different LUT is assigned to each of the six monochrome inputs. (for a total of six independent LUTs). It operates at the resolution of 8-bits in and 8-bits out. The Lookup Table can be used for point transfer as well as for thresholding.

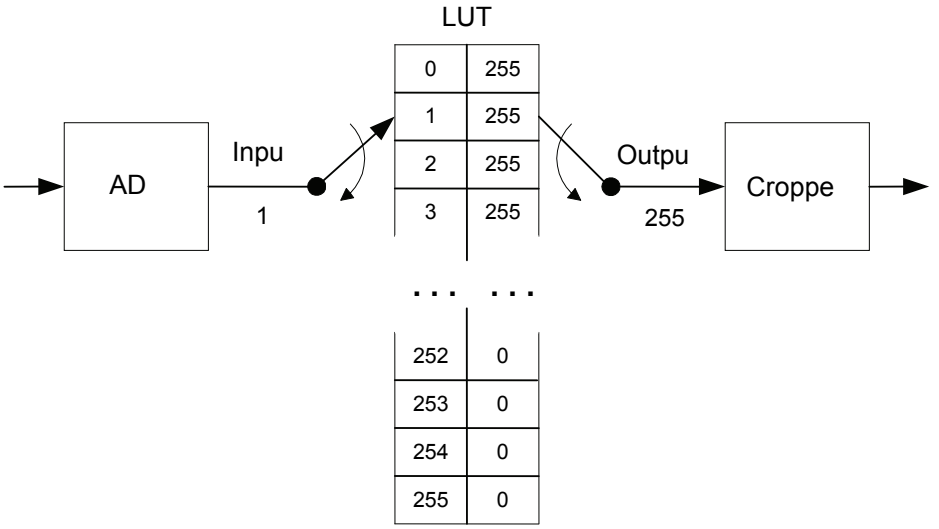


Figure 29: Lookup Table Example

Sapera parameters for Lookup Table:

CORACQ_PRM_LUT_ENABLE = {TRUE, FALSE}

CORACQ_PRM_LUT_FORMAT = CORACQ_VAL_OUTPUT_FORMAT_MONO8

CORACQ_PRM_LUT_MAX = 1

CORACQ_PRM_LUT_NENTRIES = 256

CORACQ_PRM_LUT_NUMBER = 0

Use **CorAcqSetLut()** to load a LUT into PC2-Vision.

CamExpert does not provide direct access to these parameters. They must be activated programmatically from your Sapera application via the SapLut class.

IFC parameters for Lookup Table:

P_INPUT_LUT1_FILE: filename for LUT

Cropper

The Cropper extracts a window from the incoming image. This window is represented by a rectangle where the upper-left corner is given by horizontal and vertical offset from the start of valid video and the rectangle size by width and height parameters. See below for diagram. Note that image widths must be a multiple of four bytes. For interlaced scan camera, image heights must be a multiple of two lines.

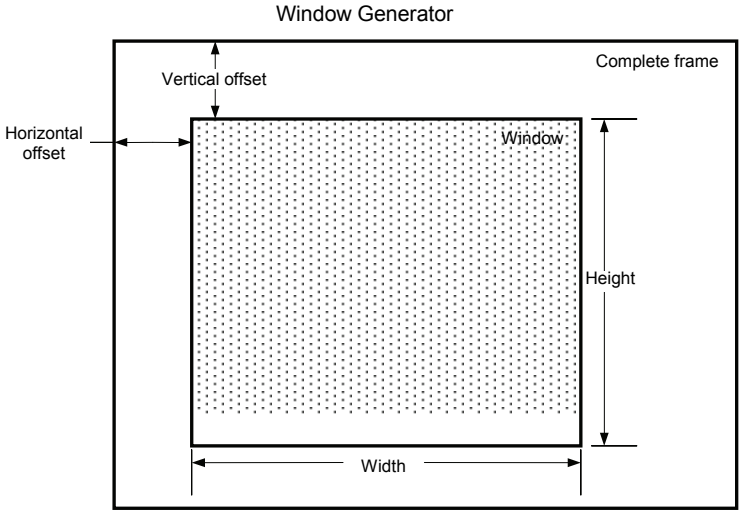


Figure 30: Window generator

Most of the time, the Cropper is configured to let the whole image pass through, that is no special region of interest is defined. This means the horizontal and vertical offset are left to their default value of 0.

Partial Scan Mode

Partial Scan mode reduces the number of lines output by a camera in order to increase the frame rate. PC2-Vision sees the output of a partial scan camera as an image with reduced height. One simply needs to adjust the frame rate (vertical sync frequency) and image height in order to acquire from a partial scan mode camera.

Sapera Parameters for Cropper:

CORACQ_PRM_CROP_LEFT: Horizontal offset

CORACQ_PRM_CROP_HEIGHT: Vertical height of area of interest

CORACQ_PRM_CROP_TOP: Vertical offset

CORACQ_PRM_CROP_WIDTH: Horizontal width of area of interest

In CamExpert, these parameters are located under the 'Image Buffer and AOI Parameters' tab.

IFC Parameters for Cropper:

P_HORZ_OFF: Horizontal offset

P_WIDTH_PIXELS: Horizontal width of area of interest

P_VERT_OFF: Vertical offset

P_HEIGHT_PIXELS: Vertical height of area of interest

Decimator

Decimation is performed horizontally and vertically by a factor of two, four, or eight. Decimation is useful in reducing memory consumption, lowering PCI bandwidth usage as well as being an easy way to scale an image. Note that horizontal and vertical decimation work independently of each other.

Horizontal decimation is accomplished by dropping pixels. See below for diagram. Only the first pixel of each pair is kept for a horizontal decimation factor of 2.

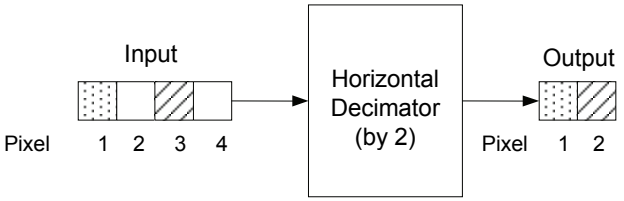


Figure 31: Horizontal decimator

Note: Horizontal decimation can be used to lower the effective pixel clock sampling rate below 7MHz. To perform this, double the pixel clock rate and activate horizontal decimation. This allows an application to grab with a pixel clock as low as 3.5 MHz.

Vertical decimation is performed by dropping lines. See below for diagram. Only the first line of each pair is kept for a vertical decimation factor of 2.

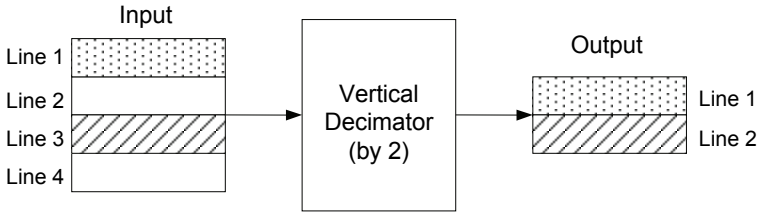


Figure 32: Vertical decimator

IFC Support for Decimator:

Use CICamera::SetZoom().

Onboard Memory

The onboard memory behaves as a temporary buffer between the camera interface and the host PCI-bus system. The total onboard memory capacity is 8MB. There is a maximum frame size of 2K x 2K for monochrome data or 1K x 1K for RGB. Two frames can be securely stored within onboard memory for double buffering. Total bandwidth to onboard memory is 320MB/second (40MHz x 4 bytes x 2 directions (IN/OUT)). Onboard memory allows the capture from cameras requiring a bandwidth exceeding the PCI theoretical maximum of 132MB/second.

The following pixel formats are supported in onboard memory:

1. 32-bit packed (for single monochrome camera)

pixel 4		pixel 3		pixel 2		pixel 1	
31	24	23	16	15	8	7	0

2. 32-bit zero padded (for three genlocked cameras as well as RGB). This pixel format allows planar transfer (see Planar Converter section on page 57).

0		CAM3 or R		CAM 2 or G		CAM1 or B	
31	24	23	16	15	8	7	0

YCrCb Engine

The YCrCb Engine converts an 8-bit monochrome image into a 16-bit padded YCrCb image to display in overlay (Windows secondary surface). The engine places the value 0x80 in chrominance. This value is added during the PCI transfer to free onboard memory from chrominance data. Furthermore, the YCrCb Engine eliminates CPU involvement when copying host buffers into display by transferring directly into overlay, bypassing the CPU.

YCrCb Engine is only available for monochrome cameras.

Sapera Support for YCrCb Engine:

YCrCb engine is not supported in current version of PC2-Vision Sapera driver.

IFC Support for YCrCb Engine:

Create an image connection using `IfxCreateImgConn()` with the flag IFC_YCRCB_SINK or use IfxCreateImgSink() with the YCRCB_SINK flag.

Planar Converter

The Planar Converter extracts RGB color components into three different buffers during PCI transfer to facilitate image processing (see the diagram below). It can also be used with three genlocked monochrome cameras.

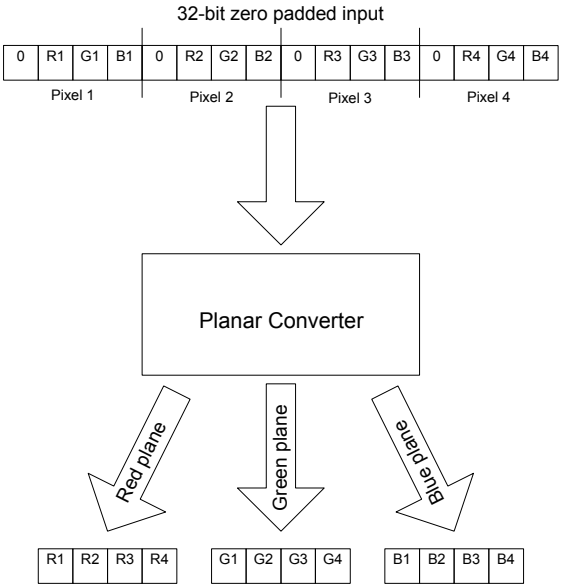


Figure 33: Planar converter

Sapera parameters for Planar Converter:

CORACQ_PRM_CAMSEL: Index of camera selector to take timing from.

CORACQ_PRM_PLANAR_INPUT_SOURCES: Flag indicating input sources to simultaneously acquire from. Bit 0 represents video1, bit 1 represents video 2 and so on.

Note: In Sapera, the planar converter is used to acquire from up to 3 genlocked monochrome cameras.

In CamExpert, these parameters are located under the 'Multi-Camera Control Parameters' tab.

IFC parameters for Planar Converter:

P_PIXEL_COLOR = IFC_RGB_PLANAR

P2V_PLANAR_MODE = {P2V_PLANAR_DISABLED, P2V_PLANAR_HORZ, P2V_PLANAR_VERT}

When using the grab option IFC_GOPT_PLANAR_INIT, CICamera::Grab must be called to start three concurrent grabs on all three channels offered by one connector. The acquisition does not actually start until the third CICamera::Grab call is made.

PCI Controller

The PCI controller has scatter-gather support to reduce CPU usage to a minimum. It retrieves a buffer descriptor list from host memory. It also supports packed data and planar data. Each color component can have a different scatter/gather list in RGB. This is also true for three genlocked cameras.

The PCI controller can sustain an average transfer rate up to 100 MB/second with bursts of 132 MB/second.

Parallel I/O

PC2-Vision provides digital I/O capability for controlling or monitoring external events. The digital input and output lines, which are available on a 26-pin header at the top of the board, can be cabled to a 25-pin D-Sub connector that occupies an open slot in the PC chassis. The functionality of the I/O port is as follows:

- IN(7-0): Eight digital TTL input lines provide capability to read these as either raw or latched (by STROBE_I) inputs. Each input pin can generate a dedicated interrupt (programmable edge).
- OUT(7-0): Eight digital TTL output lines driven by a programmable register.
- STROBE_I: Input strobe signal can be used to latch the 8-bit input data (if this mode is selected). The polarity of STROBE_I is programmable.
- STROBE_O: Output strobe signal is an output line under software control.
- I/O_INT: An interrupt input line that can be used to generate an interrupt (programmable edge)

Refer to "J3: Parallel I/O 26-Pin Dual-Row Connector" section (on page 74) for the pinout of this connector. A bracket assembly (part number 4816) is available to cable the Parallel I/O pins to a female DB25.

The Parallel I/O is backward compatible with PCVision and it has the ability to provide power to an external box: 2 dedicated 5V, 500mA power pins (with fuse protection) are available.

The Parallel I/O is achieved using HCT244 drivers with the following electrical characteristics. Note that this is a 5V TTL device.

Electrical parameters	Description	Value
$V_{IH\ min}$	Minimum high-level input voltage	2V
$V_{IL\ max}$	Maximum low-level input voltage	0.8V
$V_{I\ max}$	Maximum input voltage	5.5V
$I_{OH\ max}$	Maximum high-level output current	-6mA (sourcing)
$I_{OL\ max}$	Maximum low-level output current	6mA (sinking)

Sapera support for Parallel I/O:

Access to Parallel I/O is achieved using members of the SapGio class. Refer to *Sapera++ Programmer's* manual for a complete description of the SapGio functions.

The resource indexes for the Parallel I/O are:

0: 8-bit output resource

1: 8-bit input resource

2: 1-bit interrupt resource

Example:

```
// Assert output pin 0 of Parallel I/O
m_pGioOutput = new SapGio(SapLocation("PC2-Vision_1", 0));
m_pGioOutput->Create();
m_pGioOutput->SetPinConfig(dwBitScan, SapGio::PinOutput);
m_pGioOutput->SetPinState (0, SapGio::PinHigh);
```

Note: Sapera LT 5.10 does not support the input strobe and output strobe pins.CamExpert does not provide direct access to the I/O. It must be activated programmatically from your Sapera application using the SapGio class.

IFC Support for Parallel I/O:

Access to Parallel I/O is achieved using members of the CICapMod class:

CICapMod::InportInterruptPolarity

CICapMod::InportMode

CICapMod::InportVal

CICapMod::OutportStrobeVal

CICapMod::OutportVal

Under IFC, each input pin of the parallel I/O has an associated interrupt event:

-P2V_INTR_DATAPIN0

-P2V_INTR_DATAPIN1

-P2V_INTR_DATAPIN2

-P2V_INTR_DATAPIN3

-P2V_INTR_DATAPIN4

-P2V_INTR_DATAPIN5

-P2V_INTR_DATAPIN6

-P2V_INTR_DATAPIN7

Acquisition Interrupts

The PC2-Vision frame grabber provides acquisition interrupts that allow an application to accurately monitor acquisition status, one of the many elements that make up the "trigger-to-image reliability" model supported by PC2-Vision and its *Acquisition and Control Unit* (ACU). See "Trigger To Image Reliability" section (on page 69).

These interrupts are grouped into four families representing each acquisition stage:

- Trigger Interrupt
- Start of Image from Camera
- End of Image Capture
- End of PCI Transfer

The following block diagram illustrates the acquisition process and indicates at which stage each interrupt occurs.

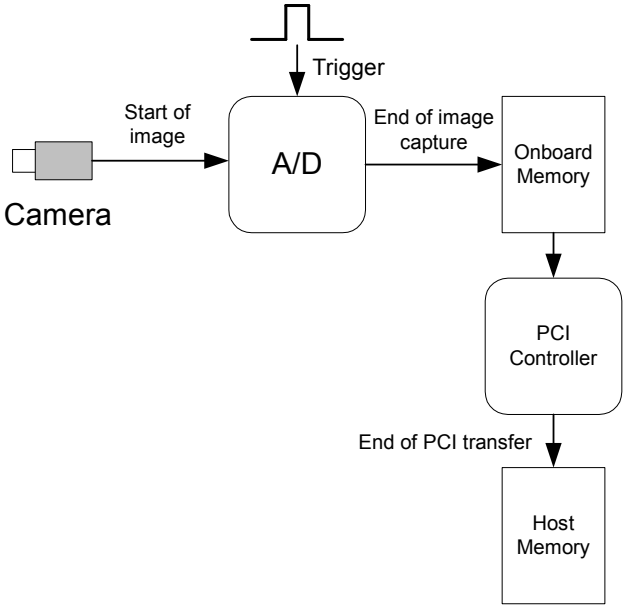


Figure 34: Acquisition interrupts

Under IFC, an interrupt event object is created using the *IfxCreateInterrupt*() global scope function. This returns a pointer to a *CInterrupt* object that is used to manage interrupts. Refer to the IFC-SDK™ Software Manual for more information using *CInterrupt* objects.

Interrupt-related Definitions

Interrupt	An interrupt is an electrical signal sent by the PC2-Vision board to the computer CPU to indicate an event on the frame grabber. The PC2-Vision driver has excellent reaction time to interrupts since interrupts are processed inside an interrupt service routine (ISR) at kernel level.
Event	An event is a WIN32 object that can take two states: signaled and non-signaled. It is used for thread synchronization. In this context, an event is associated with an interrupt so that a WIN32 thread can be unblocked when the event it is waiting for gets signaled. For example, when an interrupt is received, the corresponding event is signaled and the thread waiting for this event resumes execution.
Interrupt event object	Under IFC, an interrupt object is an IFC virtualization of an event associated to an interrupt.

Start of Trigger

The Start of Trigger interrupt is generated when the external trigger pin is asserted, usually indicating the start of the acquisition process. In IFC, this is represented by P2V_INTR_SOT. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER.

On PC2-Vision, the external trigger is protected by an opto-coupler; therefore, a minimum pulse width of 10µs is necessary to detect an active high trigger pulse while a minimum pulse width of 50µs is required for an active low trigger pulse. The PC2-Vision is also equipped with debouncer circuitry that allows the user to define the minimum acceptable pulse width programmatically.

Note: There is no Start of Trigger interrupt for a software trigger. This particular interrupt is only asserted for a pulse on the external trigger pin.

Start of Image from Camera

The Start of Image interrupt family indicates a vertical sync has been detected. Note that this does not necessarily mean the image will be captured. For instance, if you have a free-running camera at 30fps with external trigger enabled, you will get 30 interrupts per second even though the PC2-Vision waits for an external trigger to actually capture the next image. This allows the application program to count frames coming from the camera.

Start of Frame

The Start of Frame interrupt represents the beginning of a full frame output by the camera. It is asserted on the VS pulse (at the beginning of the frame). For interlaced cameras, you get one Start of Frame interrupt for each pair of fields. In IFC, this is represented by P2V_INTR_START_OF_FRAME. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_FRAME.

Start of Field

The Start of Field is only activated for interlaced scan cameras. You get a Start of Field interrupt for each incoming vertical sync (two per frame). In IFC, this is represented by P2V_INTR_START_OF_FIELD. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_FIELD.

Start of Odd Field

Start of Odd Field is only activated for interlaced scan cameras. You get a Start of Odd Field interrupt at the beginning of each incoming odd field coming from the camera. In IFC, this is represented by P2V_INTR_START_OF_ODD. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_ODD.

Start of Even Field

Start of Even Field is only activated for interlaced scan cameras. You get a Start of Even Field interrupt at the beginning of each incoming even field coming from the camera. In IFC, this is represented by P2V_INTR_START_OF_EVEN. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_START_OF_EVEN.

Note: For reasons of performance, each Start of Image interrupt is only enabled if a user function has been registered to process them.

End of Image Capture

The End of Image interrupt family is asserted when image capture is completed and data is available in onboard memory.

End of Frame

An End of Frame interrupt is generated when the last pixel from the image has been acquired and transferred to onboard memory. In IFC, this is represented by P2V_INTR_EOFRM. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_FRAME.

End of Field

The End of Field is only activated for interlaced scan cameras. You get an End of Field interrupt when the last field has been acquired and transferred into onboard memory. In IFC, this is represented by P2V_INTR_VB. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_FIELD.

End of Odd Field

The End of Odd Field is only activated for interlaced scan cameras. You get an End of Odd Field interrupt when the odd field has been acquired and transferred to onboard memory. In IFC, this is represented by P2V_INTR_ODD_VB. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_ODD.

End of Even Field

The End of Even Field is only activated for interlaced scan cameras. You get an End of Even Field interrupt when the even field has been acquired and transferred to onboard memory. In IFC, this is

represented by P2V_INTR_EVEN_VB. In Sapera, this is represented by CORACQ_VAL_EVENT_TYPE_END_OF_EVEN.

End of PCI transfer

The End of PCI transfer interrupt is generated when each frame/field has been transferred to host memory.

In Sapera, CORXFER_PRM_EVENT_TYPE provides the various transfer events. The following are available on PC2-Vision:

- CORXFER_VAL_EVENT_TYPE_END_OF_FRAME
- CORXFER_VAL_EVENT_TYPE_END_OF_FIELD
- CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER

On IFC, a different PCI transfer interrupt is available for each of the three AD channels.

Cameras	IFC Designation
Cameras 1 and 4 (blue channel)	P2V_INTR_BMDONE
Cameras 2 and 5 (green channel)	P2V_INTR_BMDONE2
Cameras 3 and 6 (red channel)	P2V_INTR_BMDONE3

Note: In IFC, most applications use the GrabWaitFrameEx() member function of the CICamera class in order to wait for the end of transfer to host memory.

When performing a planar transfer, an application receives a different interrupt for each of the three color planes (red, green, and blue).

For a progressive scan cameras, only one bus master done interrupt is received. For an interlaced scan camera, each field has its own bus master done interrupt.

Timing Diagrams

The following diagram illustrates the exact location in time for each of the interrupts previously described. An interlaced scan camera is shown since it can generate all acquisition interrupts.

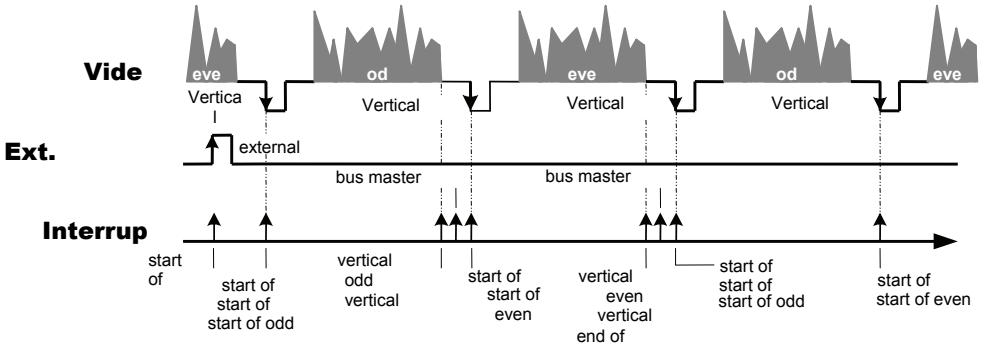


Figure 35: Acquisition Interrupts

Note: The Bus Master Done interrupt location is dependant upon PCI bus traffic as well as the size of the vertical front porch. It, therefore, may occur after the vertical sync of the next field/frame.

Error Support Interrupts

PC2-Vision supports a number of interrupts generated when problematic conditions occur within the system. These interrupts are used to notify applications that something erroneous occurred. Error Support Interrupts are part of the "trigger-to-image reliability" support.

Skipped Field

The skipped field condition is signaled when onboard memory is full resulting in the currently acquired frame being discarded.

A typical cause of this problem is an insufficient PCI bandwidth. Maximal theoretical bandwidth of the PCI bus is 132MB/second. If many bus master PCI devices are active simultaneously, it is possible that not enough bandwidth is left for PC2-Vision's PCI controller.

Another possible cause could be a high bandwidth RGB camera. PC2-Vision supports pixel clocks up to 40MHz. When using 32-bit padded data from an RGB camera, the maximal acquisition rate can reach 160MB/second. (40MHz x 4 bytes). Using asynchronous reset, this acquisition rate can be buffered by onboard memory, as long as the rate of the external trigger allows an average PCI bandwidth of about 80MB/second. In free-running mode, however, PC2-Vision will not be able to sink the 160MB/second. into the PCI bus. Note that this depends on the duration of the blanking period (since no data is digitized during blanking). One can use the Cropper or the Decimator to accommodate a high-bandwidth RGB camera. Planar transfer can also be an option as it only uses 75% of the bandwidth required for 0-padded 32-bit RGB value.

Loss of Sync

Loss of Sync is a condition that happens when PC2-Vision does not detect an HS signal coming from the currently selected camera. This typically happens when the camera cable is disconnected. When this condition is detected, image acquisition is stopped until an HS is received. Loss of Sync is also signaled if horizontal line is too short, that is, if two HS pulses are too near to each other.

Fast Camera Switching

PC2-Vision supports a Fast Camera Switching mode permitting efficient use of the six inputs by its triple-channel ADC. Fast camera switching proceeds in two steps:

1. Defines the sequence of cameras to be cycled through. No actual grab takes place during this sequence definition.
2. Starts the fast camera switching acquisition.

Note: Fast Camera Switching is not supported in Sapera LT 5.10. Use manual camera switching (that is, modifying the camera selector parameter to switch between cameras). A demo of manual camera switching is provided with the Sapera LT driver.

Note: All cameras in the switching group must have the same camera configuration file. Failure to do so may result in erratic grab or stop the grab altogether.

Best switching performance is achieved with genlocked cameras. In this case, the PC2-Vision can switch within the vertical blanking to reach maximal frame rate (all cameras have their vertical blanking aligned). This is not the case for asynchronous cameras; in this case, after switching to the next camera, PC2-Vision must wait for the VS before capturing the next frame.

Note: IFC requires the use of a single ring of buffers in order to achieve frame rate switching.

Genlocked Cameras

Genlocking cameras is generally achieved using the Master Mode capabilities of the PC2-Vision. In this scenario, the frame grabber drives the HD and VD line to all cameras. The output timing of all cameras is thus aligned, enabling PC2-Vision to go from one camera to the next within the vertical blanking and therefore not skipping any frames. Refer to the "Internal Sync" section (page 32) for a complete description of Master Mode setup.

The following diagram illustrates a group of two genlocked cameras. Because cameras are genlocked, their synchronization pulses are aligned. The internal synchronization capability of PC2-Vision prevents the PLL from unlocking, ensuring a stable image with minimal pixel jitter.

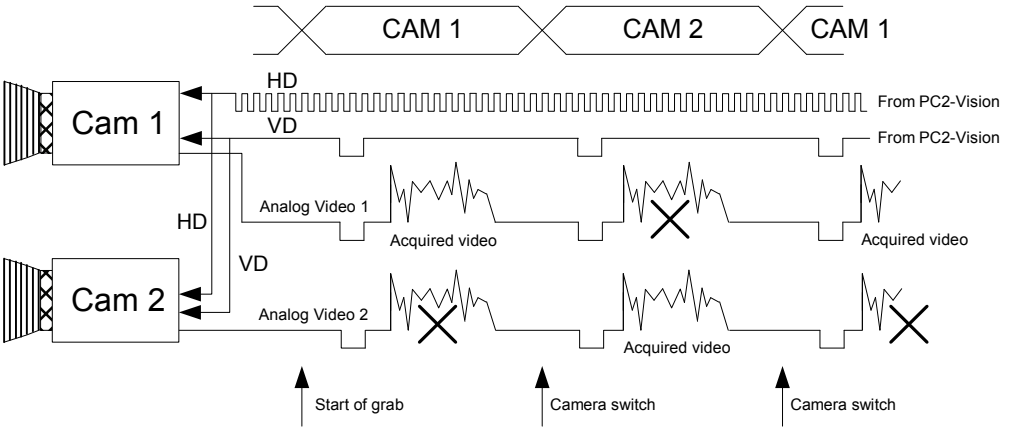


Figure 36: Fast Camera Switching for Free-Running Genlocked Cameras

Genlocking can be used for free-running or asynchronous reset mode cameras. The acquisition rate for free-running cameras is determined by the vertical sync pulse rate. For asynchronous reset mode, this rate depends on the exposure time and on the time it takes to transfer analog video signals from the camera CCD.

Example 1: Free-running genlocked cameras

- Six free-running RS-genlocked cameras @ 30fps.
- Cameras connected as two groups of three cameras (J1 controls the first group, J2 controls the second)

In this scenario, the PC2-Vision is able to acquire simultaneously from the first group of three cameras and switch to next group of three during vertical blanking. Total frame rate, therefore, is 90fps (three cameras x 30fps), or 15fps per camera.

Example 2: Edge pre-select

- Three 30fps cameras configured in edge-pre-select
- Integration period of 1/100 seconds
- Each camera receives frame reset and HD from the PC2-Vision

Acquisition time is the sum of the exposure (1/100 seconds) and the analog video transfer (1/30 seconds). This gives about 43.3ms. For most environments using asynchronous reset, an external trigger will dictate the rate of acquisition.

Asynchronous Cameras

Each camera of an asynchronous group has its own timing. They are out of phase with respect to each other. This means after switching to the next camera, the PC2-Vision must resynchronized (PLL must lock in phase with the new camera) and then wait for the VS to capture the next valid image. This overhead leads to a lower frame rate when compared to the genlocked case. As such, it is always better to use genlocked cameras when acquisition rate is an issue.

To better illustrate the difference between genlocked cameras and PLL mode camera switching, consider two free running asynchronous camera (typically two RS-170). Since the cameras are not genlocked, their frames are not in phase. This means that after grabbing from the first camera and switching to the second, the PLL must relock and then wait for the next VS (next valid frame). The same phenomenon applies when switching back to the first camera. In theory, if the PLL relocks instantly, the average frame rate would be 2/3 of the nominal frame rate; that is, a total of 20 frames per second for two 30fps cameras (10fps per camera). This is illustrated in the figure below.

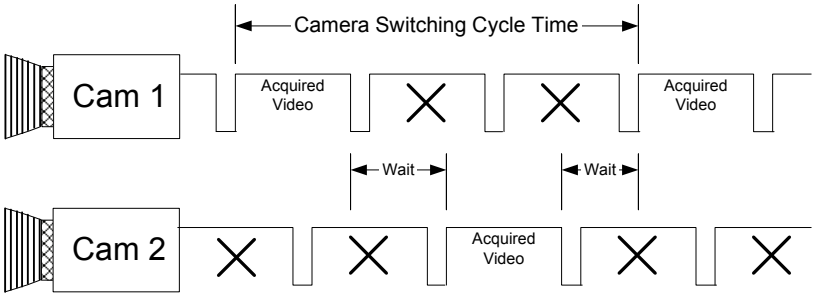


Figure 37: Asynchronous cameras fastest theoretical switching

In practice, the PLL needs to relocked before capturing the next valid frame. This further reduces the frame rate below 2/3 of its nominal value.

IFC Support for Fast Camera Switching:

IFC support fast camera switching through the following CPCVision2 member functions:

SwitchCameraDefineStart: Start definition of a sequence of camera switching grab

SwitchCameraDefineEnd: End definition of a sequence of camera switching grab

SwitchCameraGrab: Start a defined switching camera grab

SwitchCameraFreeze: Freeze a switching camera grab

Frame Delay Readout Support

Frame Delay Readout is a special mode of operation available on certain cameras that allows simultaneous acquisition from multiple cameras using a single channel ADC. This is an easy way to concurrently capture from up to six cameras using the PC2-Vision.

Note: Frame Delay Readout is not supported in Sapera LT 5.10.

Operation of Frame Delay Readout is straightforward. The frame reset pulse is sent to all cameras at the same time, thus triggering simultaneous acquisition. Once the exposure period is over, PC2-Vision selects the first camera and fires a VD pulse. The first camera outputs its analog video signal. Once the first camera signal has been digitized, PC2-Vision switches to the next camera and sends it a VD pulse. This process continues up to the last camera.

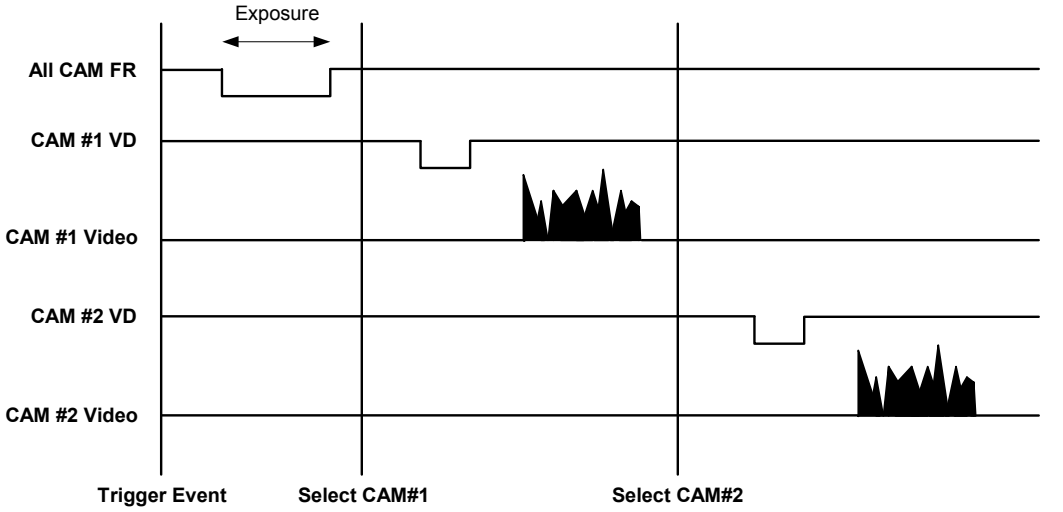


Figure 38: Frame Delay Readout

When building a system with Frame Delay Readout, consult your camera manufacturer's datasheet for any restrictions concerning this mode of operation.

Setting up the Frame Delay Readout is as simple as creating a list of cameras associated with an external trigger. All cameras must have the same camera configuration file. The list is first registered before being triggered for acquisition. A different list can be separately created for both external triggers and a third list for the software trigger.

Note: In Frame Delay Readout, IFC camera configuration files must use "Master HSync Enable = IFC_ENABLE" and "Source of Input Sync = P2V_SYNC_INTERNAL_SYNC".

IFC Support for Frame Delay Readout:

IFC support frame delay readout through the following CPCVision2 member functions:

SetFrameDelaySequence: Define the sequence of cameras for a frame delay acquisition

FrameDelaySnap: Perform a frame delay snap on a set of cameras

FrameDelayWait: Wait for a frame delay snap to complete

Trigger To Image Reliability

Trigger-to-image reliability incorporates all stages of image acquisition inside an integrated controller to increase reliability and simplify error recovery. The trigger to image reliability model fuses together all the elements required to acquire images so that a central unit manages them coherently. These elements include, among others, I/O to control timing to the camera, onboard memory to compensate for PCI bus latency and error notification. Whenever PC2-Vision detects a problem, the user application is immediately informed and can take appropriate action to return to normal operation. PC2-Vision offers this robustness through its ACU (Acquisition and Control Unit), which manages all six frame grabber inputs and monitors in real-time the acquisition state of each input. As such, it is transparent to user applications for the most part.

On PC2-Vision, user application can interact with trigger-to-image through the following:

- Glitches on the external trigger line are debounced by the ACU. A parameter is available to indicate the minimal pulse duration to consider an external trigger pulse valid. Refer to "External Trigger" (on page 41) for more information.
- For each frame/field, a number of interrupts are generated to indicate the following events:
  - a) Trigger interrupt
    b) Start for frame/field interrupt
    c) End of frame/field interrupt
    d) End of transfer interrupt
- By monitoring these events, it is possible to know the flow of acquisition of the system as demonstrated in "Acquisition Interrupts" section (on page 60).
- If something goes wrong during the acquisition process, a notification is sent for the following:
  - a) Field skip:
    This happens when PCI bandwidth is limited or onboard memory is full (8MB of onboard memory on PC2-Vision). Frame being acquired is discarded.
    b) Loss of Sync:
    This event represents a mismatch between the expected camera configuration and what is sent by the camera. This means the image received by the frame grabber is smaller than expected or no horizontal synchronization is received from the camera. Note that an image larger than expected is compensated by the Cropper, so you will not get a bad synchro interrupt.

    Refer to the "Error Support Interrupts" (on page 64) for more information on this topic.

The rest of trigger-to-image is handled internally by the ACU to correctly synchronize acquisition among the different inputs. This is done automatically and does not require user application involvement. This covers HS, VS, WEN, frame reset, external trigger, strobe signal and transfers over the PCI bus.

Technical Reference

Hardware Specifications

The following provides specific information related to PC2-Vision hardware specifications.

PC2-Vision Specifications

Function	Description
Acquisition	
	Standard RS-170 and CCIR, RGB, dual-channel and non-standard progressive scan providing composite video (non-standard progressive scan can be driven with external TTL timing: HSYNC, VSYNC, and Frame Reset)
	Six analog video inputs, AC coupled and terminated to 75Ω
	Triple 8-bit flash A/C; Input pixel rates to 40MHz
	Simultaneous capture from any three synchronized monochrome cameras
	DC Restoration – programmable clamp pulse
	Partial scan mode
	Input gain – software selectable
	Low-pass filter – software selectable
	Pixel clock from 7MHz up to 40MHz (minimum 3.5MHz using horizontal decimator)
	Programmable time-base generator and programmable resolution to 2048 x 2048 interlaced or non-interlaced

Synchronization and timing control	
	Composite sync
	Separate sync, TTL
	Pixel clock input, TTL
	Trigger input, opto-isolated TTL or RS-422
	Programmable trigger de-bounce delay from 1 to 255 microseconds
	One External Trigger input per group of three cameras; synchronizes acquisition to external events
	Programmable trigger, slow strobe, fast strobe
	One strobe output per group of three cameras
	I/O controls – 8 TTL inputs, 8 TTL outputs, Interrupt driven for immediate software response.
	Onboard RS-232 COM port for camera control (mapped as a COM port in the system)
Host transfers and data format	
	Pixel format: MONO8, YUV16, RGB32, RGB planar
	Simultaneous transfer of three camera images into host memory in a packed pixel format (C1,C2,C3,x)
	DMA engine supports transfers up to 100MB/second
	DMA engine supports scatter/gather
	DMA engine supports de-interlacing images
I/O Pins	
	I/O pins include: Parallel I/O, frame reset, VS, HS, WEN, Pixel clock, composite sync.
Onboard Processing	
	Input lookup-tables – following A/D
	Area of Interest transfers
	YCrCb converter
Power	
	Camera power onboard, +12 V @ 500mA, fused protected
	Parallel I/O power, 2-pins at +5V @ 500mA, fused protected

PC2-Vision Connector and Jumper Locations

PC2-Vision component view

The PCI Express and PCI board versions have the same component layout (except the PCI Express version does not have LED 3).

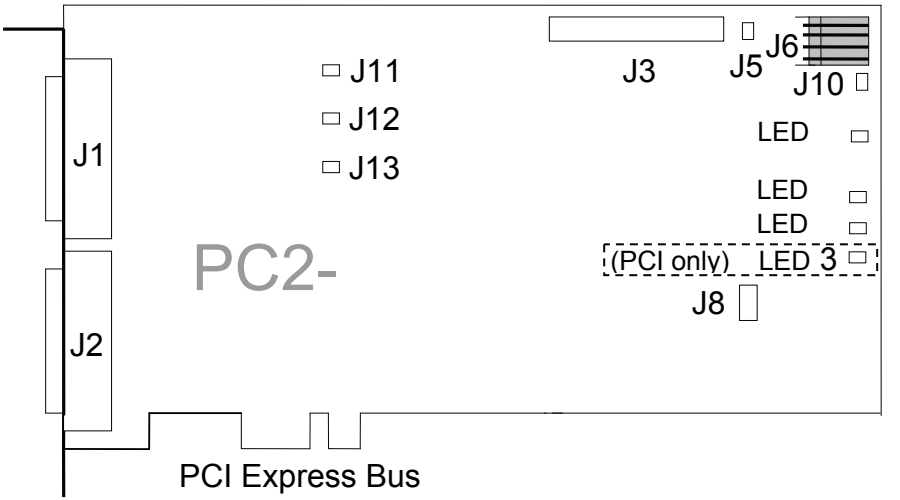


Figure 39: Component View

Connector Bracket

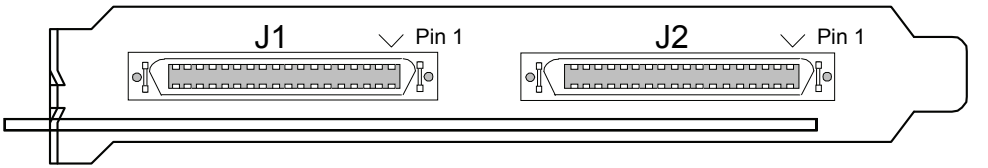
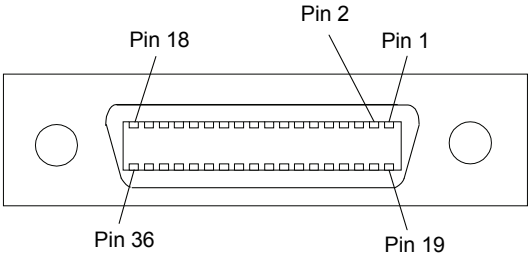


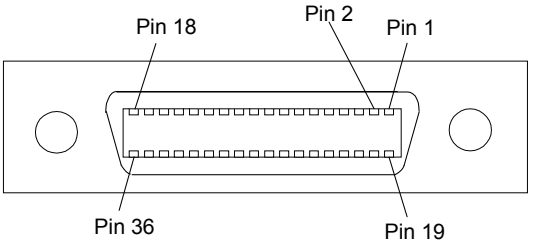
Figure 40: Connector Bracket

J1: MDR 36-Pin Female Group 1 Camera Connector



Pin #	Pin Name	Type	Pin #	Pin Name	Type
1	Video1	Input	19	Video1 AGND	
2	HS1	Input/Output	20	VS1	Input/Output
3	Camera_Trigger 1	Output	21	WEN1	Input
4	Digital GND		22	Digital GND	
5	Video2	Input	23	Video2 AGND	Input
6	HS2	Input/Output	24	VS2	Input/Output
7	Camera_Trigger 2	Output	25	WEN2	Input
8	Video3	Input	26	Video3 AGND	
9	HS3	Input/Output	27	VS3	Input/Output
10	Camera_Trigger 3	Output	28	WEN3	Input
11	Strobe1	Output	29	Digital GND	
12	Digital GND		30	+12V	
13	-CSync1	Input	31	+12V GND	
14	Reserved		32	+12V	
15	Reserved		33	+12V GND	
16	Digital GND		34	RX1	Input
17	Ext_Trig1-	Input	35	TX1	Output
18	Ext_Trig1+	Input	36	Pixel_Clk1	Input

J2: MDR 36-Pin Female Group 2 Camera Connector



Pin #	Pin Name	Type	Pin #	Pin Name	Type
1	Video4	Input	19	Video4 AGND	
2	HS4	Input/Output	20	VS4	Input/Output
3	Camera_Trigger 4	Output	21	WEN4	Input
4	Digital GND		22	Digital GND	
5	Video5	Input	23	Video5 AGND	Input
6	HS5	Input/Output	24	VS5	Input/Output
7	Camera_Trigger 5	Output	25	WEN5	Input
8	Video6	Input	26	Video6 AGND	
9	HS6	Input/Output	27	VS6	Input/Output
10	Camera_Trigger6	Output	28	WEN6	Input
11	Strobe2	Output	29	Digital GND	
12	Digital GND		30	+12V	
13	-CSync2	Input	31	+12V GND	
14	Reserved		32	+12V	
15	Reserved		33	+12V GND	
16	Digital GND		34	RX2	Input
17	Ext_Trig2-	Input	35	TX2	Output
18	Ext_Trig2+	Input	36	Pixel_Clk2	Input

J3: Parallel I/O 26-Pin Dual-Row Connector

PC2-Vision provides a digital I/O capability for controlling or monitoring external events. The digital input and output lines, available on a 26-pin header at the top of the PC card, can be cabled to a 25-pin female D-Sub connector that occupies an open slot in the chassis using a bracket assembly (part number 4816).

25	23	...	3	1
26	24	...	4	2

Header Pin #	Signal name	Description	Connector Pin #
1	GND	Digital ground	1
3	GND	Digital ground	2
5	GND	Digital ground	3
7	GND	Digital ground	4
9	IN1	Digital Input pin 1	5
11	IN3	Digital Input pin 3	6
13	IN5	Digital Input pin 5	7
15	IN7	Digital Input pin 7	8
17	OUT0	Digital Output pin 0	9
19	OUT2	Digital Output pin 2	10
21	OUT4	Digital Output pin 4	11
23	OUT6	Digital Output pin 6	12
25	+5V	+5V power output	13
2	STROBE_0	Strobe Output	14
4	STROBE_1	Strobe Input	15
6	I/O_INT	Interrupt Input	16
8	IN0	Digital Input pin 0	17
10	IN2	Digital Input pin 2	18
12	IN4	Digital Input pin 4	19
14	IN6	Digital Input pin 6	20
16	+5V	+5V power output	21
18	OUT1	Digital Output pin 1	22
20	OUT3	Digital Output pin 3	23
22	OUT5	Digital Output pin 5	24
24	OUT7	Digital Output pin 7	25
26	n/c	no connection	n/a

J4, J7, J8, J14: Reserved

Reserved.

J5: Recovery Jumper

Recovery jumper for flash update.

J6: Power Connector

J6 must be connected to a computer floppy disk power cable to provide 12V to the camera through the J1 and J2 camera connectors.

To remove the floppy disk power cable from the J6 connector, carefully lift the cable connector head from the J6 connector to unlatch the locking mechanism underneath the connector, then carefully pull cable from the board connector.

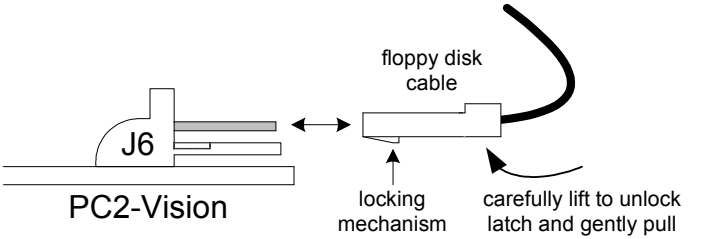


Figure 41: Removing floppy power cable

J10: Camera Power from PCI Connector

When this jumper is set, 12V power for the camera comes from the PCI connector. When this jumper is removed, the J6 power connector must be connected to a computer floppy disk power cable to provide 12V to the camera (alternatively, you can supply your own power supply to the J6 connector).

J11, J12, J13: Video Signal

These test points provide access to the video signal just before conversion by the ADC.

J11: CAM1 or CAM4

J12: CAM2 or CAM5

J13: CAM3 or CAM6

LEDs

LED1: indicates a 3.3V PCI bus.

LED2: indicates the fail-safe boot mode (when jumper J5 is removed). It is not to be turned ON during the normal operation of the board

LED3: indicates a 5V PCI bus (PCI board version only).

LED4: PCI 12V

Note: LED1 and LED3 are mutually exclusive.

Computer Requirements for the PC2-Vision

The PC2-Vision requires at minimum an Intel Pentium III or compatible computer system with a free PCI or PCI Express local bus slot, depending on your board version.

Operating System Support

- Windows XP, Windows Vista, Windows 7, Windows 8.
- 32-bit or 64-bit

PC2-Vision Physical Dimensions

Approximately 6.675" W×4.2" H (16.95 cm W×10.67 cm H)

Power Requirements

	Typical	Maximum
+ 5 Volts	3 A	5 A
+ 12 Volts	120 mA	250 mA
- 12 Volts	75 mA	100 mA

Environment

Ambient Temperature:	0° to 55° C (operation) -40° to 75° C (storage)
Relative Humidity:	5% to 95% non-condensing (operating) 0% to 95% (storage)

Camera Compatibility

Review the DALSA web page for the latest compatible camera information for the PC2 Vision at http://dalsa.com/mv/products .

Interfacing Cables

MDR-36 Connector

TELEDYNE DALSA offers a variety of camera cables for PC2-Vision (listed in the following section). To build your own camera cable, you can select MDR-36 components from 3M (http://www.3m.com).

Part Description	3M part number	3M Id
MDR-36 shielded solder plug	10136-3000VE	JE-1501-8028-7
MDR-36 plastic solder plug junction shell	10336-52F0-008	JE-1501-8040-2

Interfacing Cable Diagrams and Specifications

The following ten cables are available from DALSA to interface between the specific camera used and the PC2-Vision. For purchasing information , see "Sales Information" on page 167.

Cables	Part Number
Single camera BNC cable	OC-PC2C-V1B00
Single RGB camera BNC cable	OC-PC2C-V1B01
PCVision Series adapter cable	OC-PC2C-V3A00
Single camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V1H00
Three camera Hirose-12 cable, trigger on pin 9	OC-PC2C-V3H00
Single camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V1H01
Three camera Hirose-12 cable, trigger on pin 11	OC-PC2C-V3H01
Single camera Hirose-12 + Hirose-6 for Jai A-series	OC-PC2C-V1H02
Three camera Hirose-12 + Hirose-6 for Jai A-series	OC-PC2C-V3H02
Jai CV-M77 RGB camera cable	OC-PC2C-V1D00
Pulnix camera cable (supporting three cameras)	OC-PC2C-V3H03
Jai M-series camera cable (supporting three cameras)	OC-PC2C-V3H04

Warning: Some cameras have frame reset on their Hirose-12 pin 9 while other have it on pin 11. It is imperative to use the appropriate camera cable that matches the frame reset pinout. Failure to do so could result in board damage.

Cable 1: Standard input cable for one camera using BNC connector

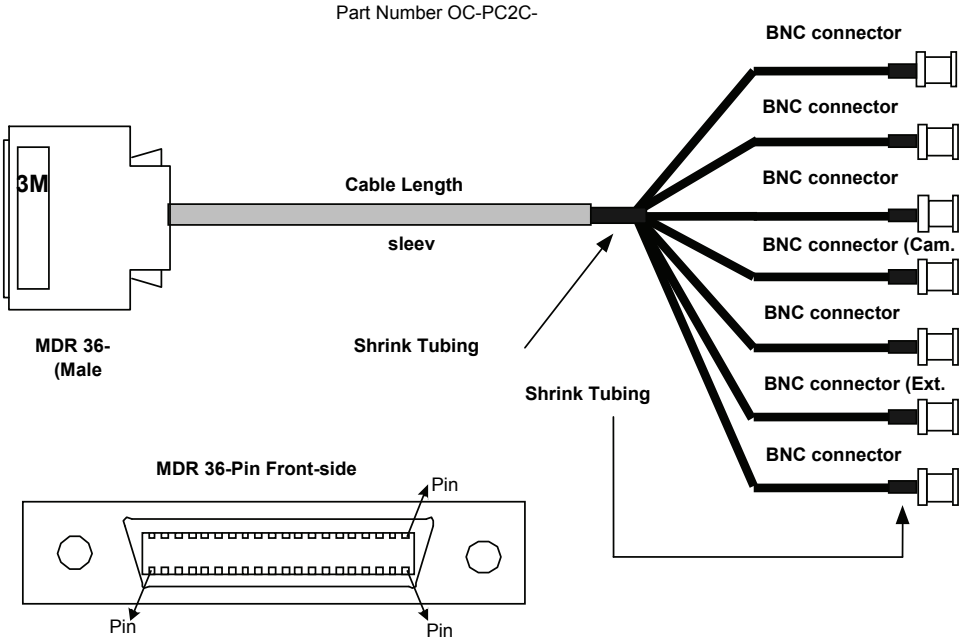


Figure 42: Single camera BNC cable

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Video
1	Video1		Coax Wire
19	Video1 AGND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: HS
2	HS1		Coax Wire
4	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: VS
20	VS1		Coax Wire
22	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Cam Trigger
3	Camera Trigger1		Coax Wire
29	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: PCLK

36	PCLK1		Coax Wire
29	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Ext. Trigger
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Strobe
11	Strobe1		Coax Wire
12	Digital GND		Coax Shield

Cable 2: Standard RGB input cable for one camera using BNC connectors

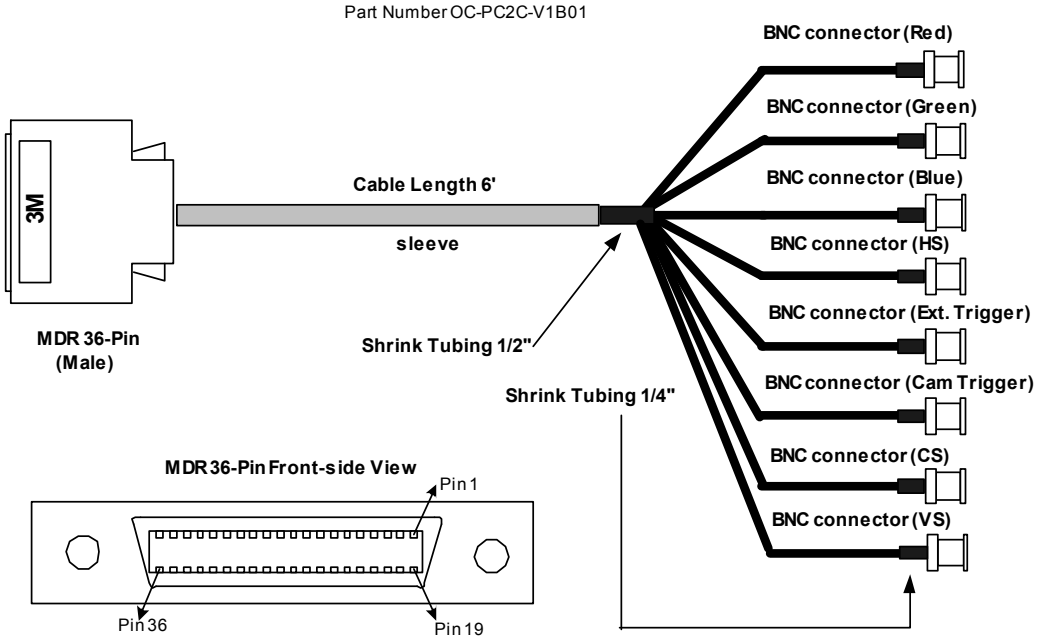


Figure 43: Single RGB camera BNC cable

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Blue
1	Blue		Coax Wire
19	Blue AGND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Green
5	Green		Coax Wire
23	Green AGND		Coax Shield
Pin	MDR 36-Pin (Male) Frame	Pin	BNC Male Connector Label: Red

#	Grabber	#	
8	Red		Coax Wire
26	Red AGND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: HS
2	HS1		Coax Wire
4	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: VS
20	VS1		Coax Wire
22	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Trigger In
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: Cam Trigger
3	Camera Trigger1		Coax Wire
29	Digital GND		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC Male Connector Label: CS
13	CS		Coax Wire
12	Digital GND		Coax Shield

Cable 3: PC2-Vision to PCVision adapter cable

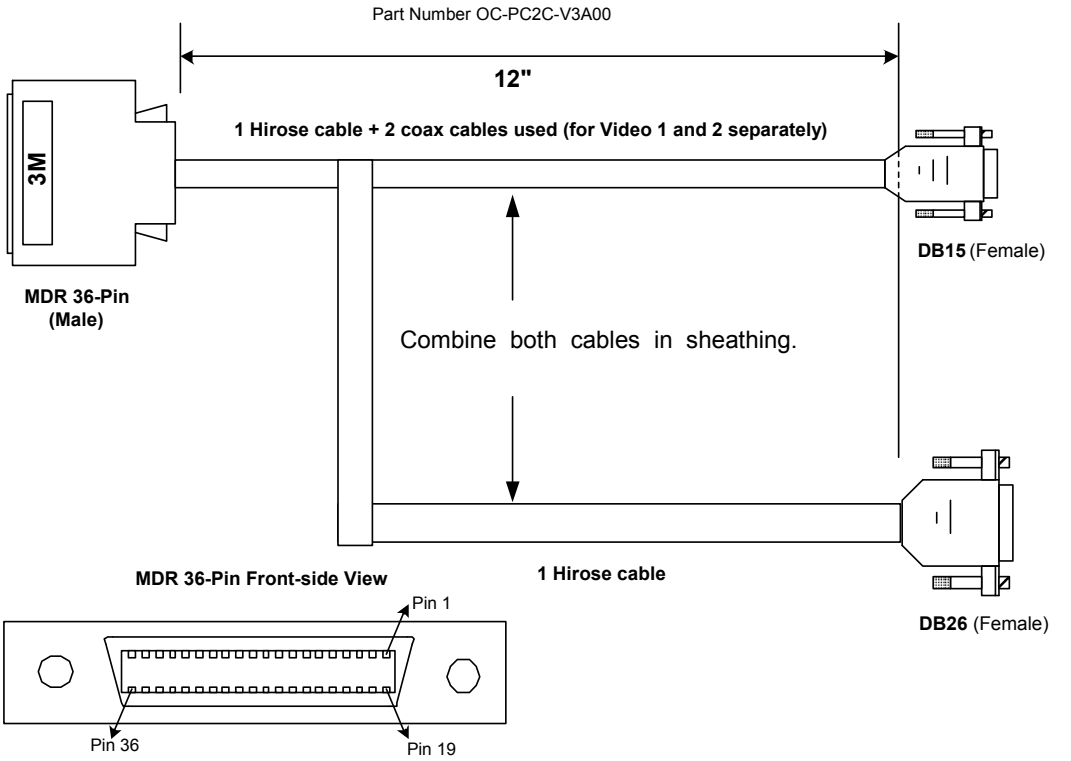


Figure 44: PCVision Series adapter cable

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	DB15 (Female)	Wire Type
1	Video1	2		Coax Cable
19	Video1 AGND	7		Coax Cable
2	HS1	13		Coax 1 Wire
4	Digital GND	5		Coax 1 Shield
20	VS1	14		Coax 2 Wire
4	Digital GND	5		Coax 2 Shield
3	Camera Trigger1	9		Wire
30	+12V	15		Wire
31	+12V GND	10		Wire
5	Video2	1		Coax Cable
23	Video2 AGND	6		Coax Cable
6	HS2	11		Coax 3 Wire
22	Digital GND	4		Coax 3 Shield

24	VS2	12		Coax 4 Wire
22	Digital GND	4		Coax 4 Shield
7	Camera Trigger2	8		Wire
Pin #	**MDR 36-Pin (Male) Frame Grabber**	**Pin #**	**DB26 (Female)**	**Wire Type**
8	Video3	2		Coax 1 Wire
26	Video3 AGND	11		Coax 1 Shield
9	HS3	21		Coax 2 Wire
29	Digital GND	3		Coax 2 Shield
27	VS3	22		Coax 3 Wire
29	Digital GND	3		Coax 3 Shield
10	Camera Trigger3	13		Coax 4 Wire
29	Digital GND	3		Coax 4 Shield
32	+12V	23		Wire
33	+12V GND	14		Wire
18	Ext_Trig1+	17		Wire
17	Ext_Trig1-	24		Jumper Wire
11	Strobe1	6		Wire
29	Digital GND	24		Jumper Wire

Cable 4: Standard interface to one Hirose 12-pin with trigger pulse on pin 9

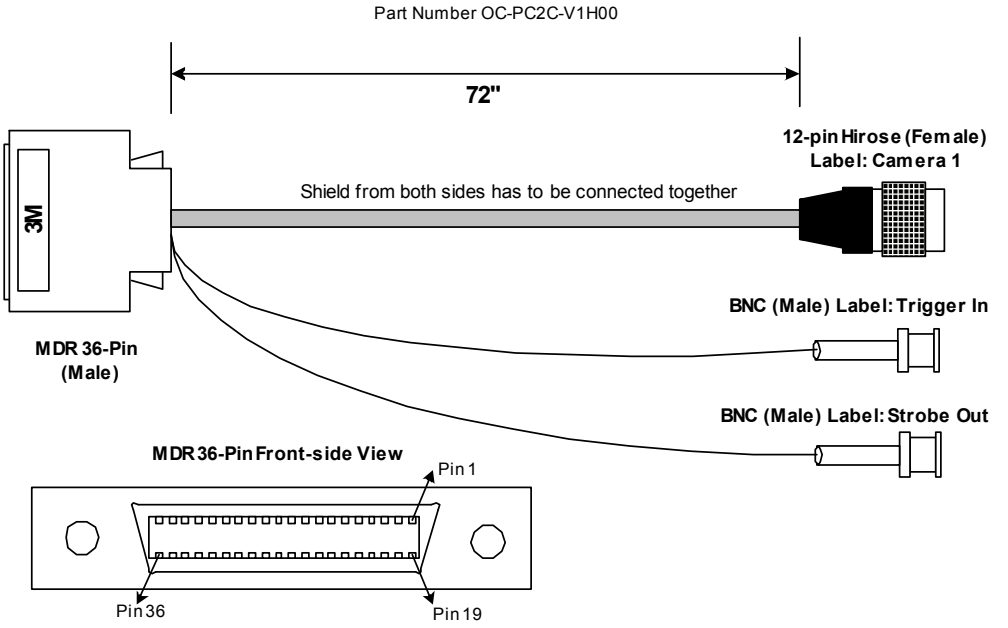


Figure 45: Single camera Hirose-12 cable, trigger on pin 9

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-pin (Female) Camera 1
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
3	Camera Trigger1	9	Coax 4 Wire
29	Digital GND	8	Coax 4 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield
11	Strobe1		Coax Wire
12	Digital GND		Coax Shield

Cable 5: Standard interface to three Hirose 12-pin connectors with trigger pulse on pin-9

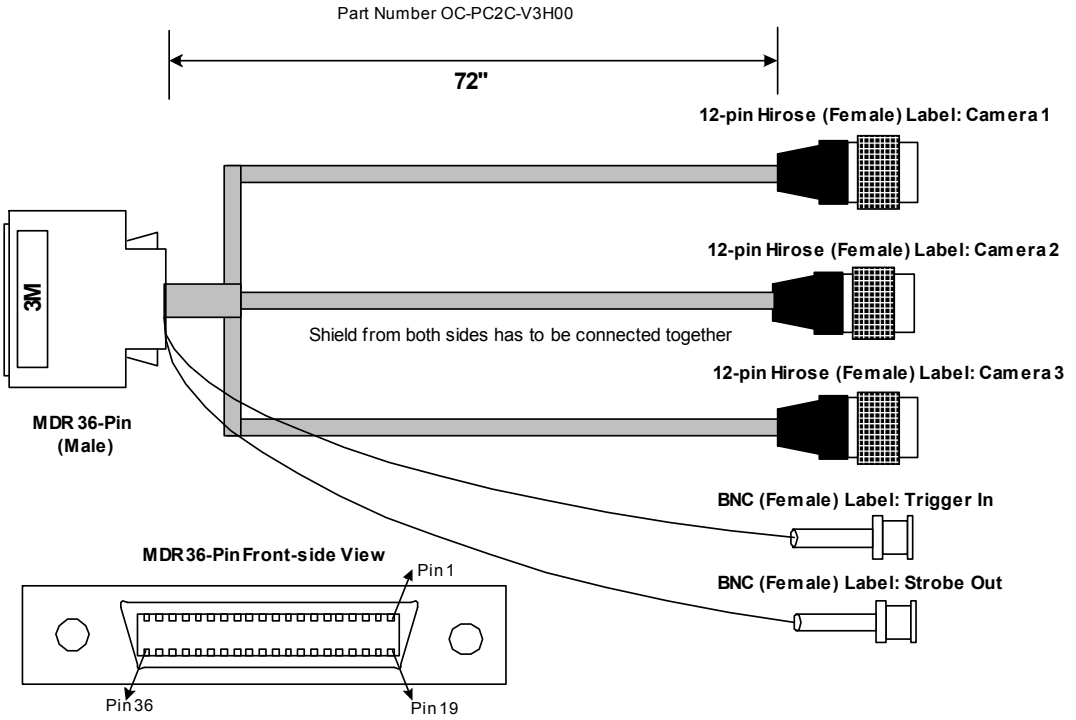


Figure 46: Three camera Hirose-12 cable, trigger on pin 9

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Camera 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female) Camera 1
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
4	Digital GND	12	Coax 3 Shield
3	Camera Trigger1	9	Coax 4 Wire
4	Digital GND	8	Coax 4 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
Camera 2			

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female) Camera 2
5	Video2	4	Coax 1 Wire
23	Video2 AGND	3	Coax 1 Shield
6	HS2	6	Coax 2 Wire
22	Digital GND	5	Coax 2 Shield
24	VS2	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
7	Camera Trigger2	9	Coax 4 Wire
22	Digital GND	8	Coax 4 Shield
32	+12V	2	Wire
33	+12V GND	1	Wire

Camera 3

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female) Camera 3
8	Video3	4	Coax 1 Wire
26	Video3 AGND	3	Coax 1 Shield
9	HS3	6	Coax 2 Wire
29	Digital GND	5	Coax 2 Shield
27	VS3	7	Coax 3 Wire
29	Digital GND	12	Coax 3 Shield
10	Camera Trigger3	9	Coax 4 Wire
29	Digital GND	8	Coax 4 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire

BNC

Pin #	MDR 36-Pin (Male) Frame Grabber	BNC (Female) Connector Trigger In
18	Ext_Trig1+	Coax Wire
17	Ext_Trig1-	Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	DALSA Connector
11	Strobe1	Coax Wire
12	Digital GND	Coax Shield

Cable 6: Standard interface to one Hirose 12-pin with WEN and trigger pulse on pin 11

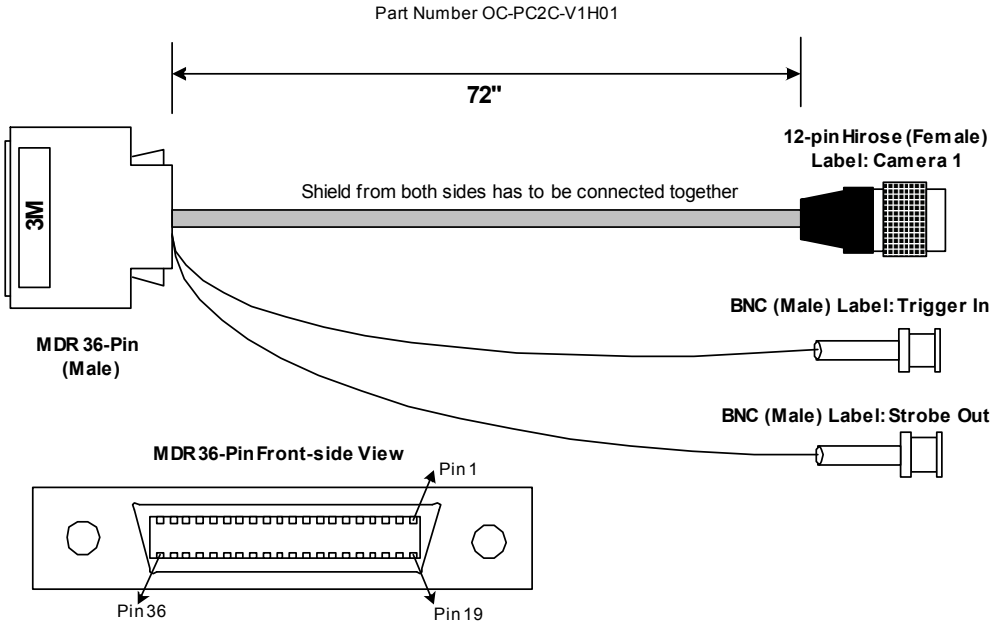


Figure 47: Single camera Hirose-12 cable, trigger on pin 11

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-pin (Female)
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
3	Camera Trigger1	11	Coax 4 Wire
29	Digital GND	8	Coax 4 Shield
21	WEN1	10	Wire
30	+12V	2	Wire
31	+12V GND	1	
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield

11	Strobe1		Coax Wire
12	Digital GND		Coax Shield

Cable 7: Standard interface to three Hirose 12-pin connectors with WEN and trigger pulse on pin-11

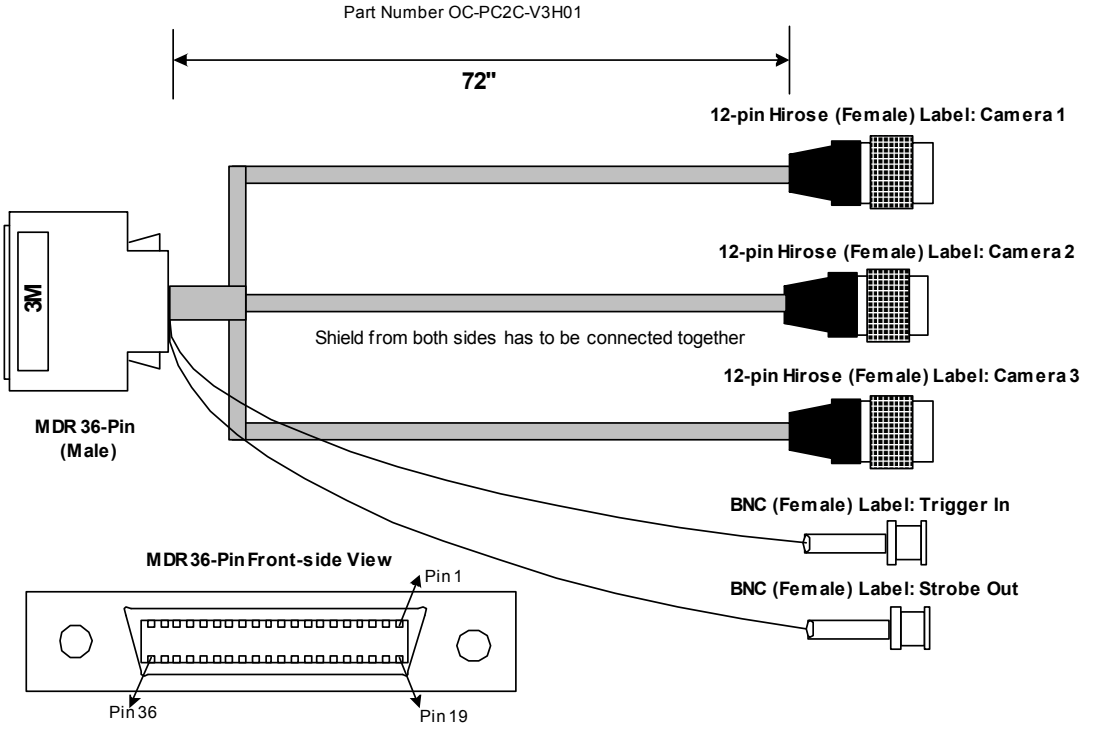


Figure 48: Three camera Hirose-12 cable, trigger on pin 11

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

Camera 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female) Camera 1
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
4	Digital GND	12	Coax 3 Shield
3	Camera Trigger1	11	Coax 4 Wire
4	Digital GND	8	Coax 4 Shield
21	WEN1	10	Wire
30	+12V	2	Wire
31	+12V GND	1	Wire
Camera 2			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female) Camera 2
5	Video2	4	Coax 1 Wire
23	Video2 AGND	3	Coax 1 Shield
6	HS2	6	Coax 2 Wire
22	Digital GND	5	Coax 2 Shield
24	VS2	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
7	Camera Trigger2	11	Coax 4 Wire
22	Digital GND	8	Coax 4 Shield
25	WEN2	10	Wire
32	+12V	2	Wire
33	+12V GND	1	Wire
Camera 3			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female) Camera 3
8	Video3	4	Coax 1 Wire
26	Video3 AGND	3	Coax 1 Shield
9	HS3	6	Coax 2 Wire
29	Digital GND	5	Coax 2 Shield
27	VS3	7	Coax 3 Wire
29	Digital GND	12	Coax 3 Shield
10	Camera Trigger3	11	Coax 4 Wire
29	Digital GND	8	Coax 4 Shield
28	WEN3	10	Wire
30	+12V	2	Wire

31	+12V GND	1	Wire
BNC			
Pin #	MDR 36-Pin (Male) Frame Grabber	BNC (Female) Connector Trigger In	
18	Ext_Trig1+	Coax Wire	
17	Ext_Trig1-	Coax Shield	
11	Strobe1	Coax Wire	
12	Digital GND	Coax Shield	

Cable 8: Standard interface for one Jai camera

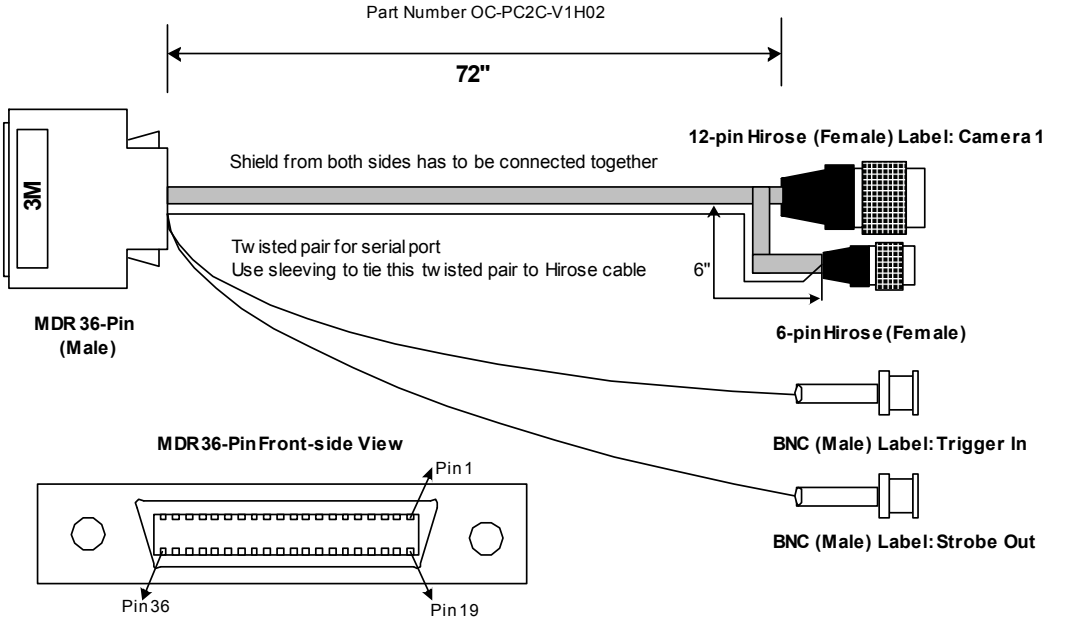


Figure 49: Single camera Hirose-12 + Hirose-6 for Jai

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

A "twisted pair" appellation refers to a separate cable used to supplement the twelve conductors on the Hirose cable. This cable must use sleeving to attach it to the corresponding Hirose cable.

Camera 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-pin (Female)
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
21	WEN1	10	Wire
30	+12V	2	Wire
31	+12V GND	1	Wire
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 6-pin (Female)
3	Camera Trigger1	5	Coax 4 Wire
29	Digital GND	4	Coax 4 Shield
34	RX1	1	Twisted pair conductor 1
35	TX1	2	Twisted pair conductor 1
BNC			
Pin #	MDR 36-Pin (Male) Frame Grabber	BNC Male Connector Label: Trigger In	
18	Ext_Trig1+	Coax Wire	
17	Ext_Trig1-	Coax Shield	
11	Strobe1	Coax Wire	
12	Digital GND	Coax Shield	

Cable 9: Standard interface for Jai cameras

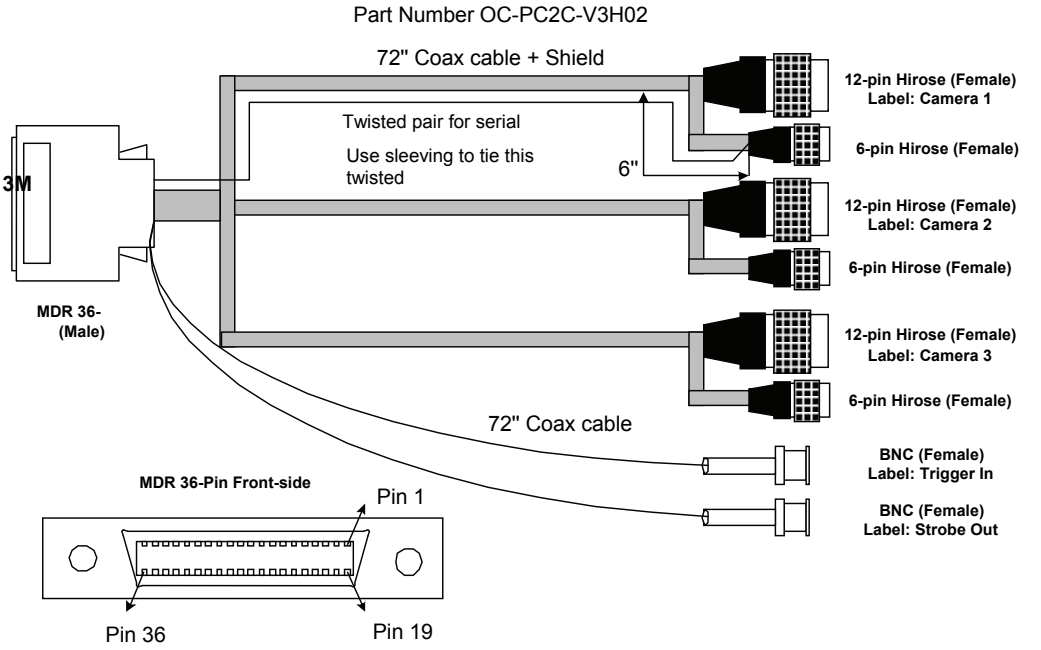


Figure 50: Three camera Hirose-12 + Hirose-6 for Jai

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

A "twisted pair" appellation refers to a separate cable used to supplement the twelve conductors on the Hirose cable. This cable must use sleeving to attach it to the corresponding Hirose cable.

Camera 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire

4	Digital GND	12	Coax 3 Shield
21	WEN1	10	Wire
30	+12V	2	Wire
31	+12V GND	1	Wire
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 6-Pin (Female)
3	Camera Trigger1	5	Coax 4 Wire
4	Digital GND	4	Coax 4 Shield
34	RX1	1	Twisted pair conductor 1
35	TX1	2	Twisted pair conductor 2
Camera 2			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
5	Video2	4	Coax 1 Wire
23	Video2 AGND	3	Coax 1 Shield
6	HS2	6	Coax 2 Wire
22	Digital GND	5	Coax 2 Shield
24	VS2	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
25	WEN2	10	Wire
32	+12V	2	Wire
33	+12V GND	1	Wire
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 6-Pin (Female)
7	Camera Trigger2	5	Coax 4 Wire
22	Digital GND	4	Coax 4 Shield
Camera 3			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
8	Video3	4	Coax 1 Wire
26	Video3 AGND	3	Coax 1 Shield
9	HS3	6	Coax 2 Wire
29	Digital GND	5	Coax 2 Shield
27	VS3	7	Coax 3 Wire
29	Digital GND	12	Coax 3 Shield
28	WEN3	10	Wire
30	+12V	2	Wire
31	+12V GND	1	Wire
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 6-Pin (Female)

10	Camera Trigger3	5	Coax 4 Wire
29	Digital GND	4	Coax 4 Shield
BNC			
Pin #	MDR 36-Pin (Male) Frame Grabber	BNC (Male) Connector Trigger In	
18	Ext_Trig1+	Coax Wire	
17	Ext_Trig1-	Coax Shield	
11	Strobe1	Coax Wire	
12	Digital GND	Coax Shield	

Cable 10: Jai CV-M77 RGB cable

Part Number OC-PC2C-V1D00

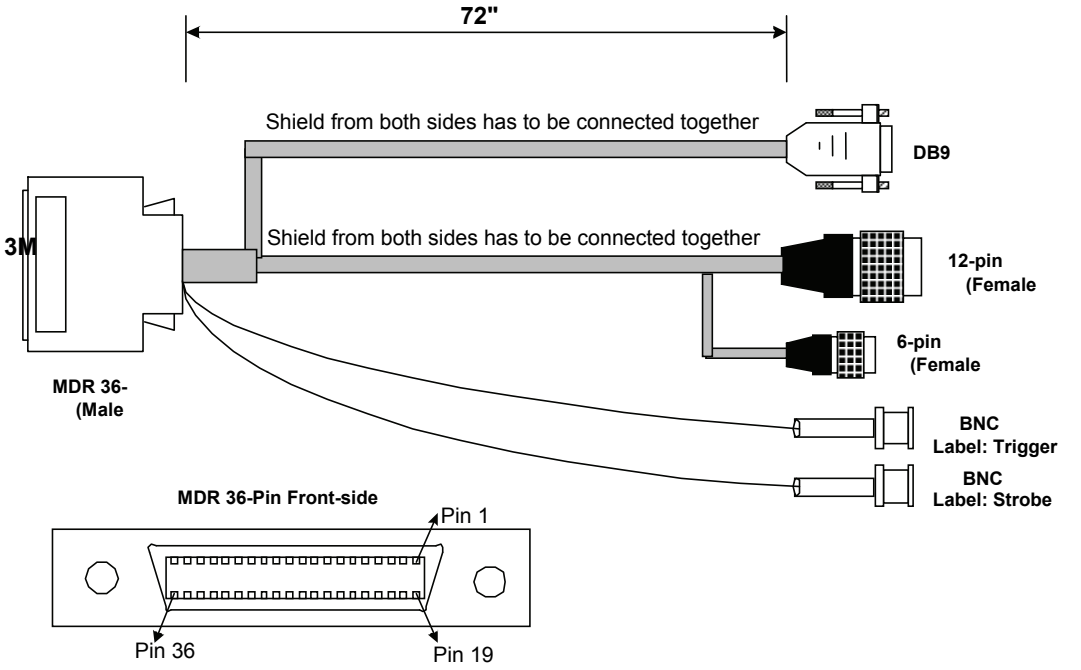


Figure 51: Jai CV-M77 RGB camera cable

Hirose Cable 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-pin Connector (Female)
2	HS1	6	Coax 1 Wire
4	Digital GND	5	Coax 1 Shield
20	VS1	7	Coax 2 Wire
22	Digital GND	12	Coax 2 Shield
21	WEN1	10	Coax 3 Wire
22	Digital GND	8	Coax 3 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 6-pin Connector (Female)
34	RX1	1	Wire
35	TX1	2	Wire
3	Camera Trigger 1	5	Coax 4 Wire
4	Digital GND	3	Coax 4 Shield
Hirose Cable 2			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	DB9 Connector (Male)
1	Video1 (Blue)	5	Coax 1 Wire
19	Video1 AGND (Blue AGND)	2	Coax 1 Shield
5	Video2 (Green)	4	Coax 2 Wire
23	Video2 AGND (Green AGND)	2	Coax 2 Shield
8	Video3 (Red)	3	Coax 3 Wire
26	Video3 AGND (Red AGND)	2	Coax 3 Shield
13	-CSync1	7	Coax 4 Wire
12	Digital G ND	8	Coax 4 Shield
Separate Coax Cables			
Pin #	MDR 36-Pin (Male) Frame Grabber	BNC Male Connector Label: Trigger In	
18	Ext_Trig1+	Coax Wire	
17	Ext_Trig1-	Coax Shield	
11	Strobe1	Coax Wire	
12	Digital GND	Coax Shield	

Cable 11: PC2-Vision Interface Cable to three PULNIX camera

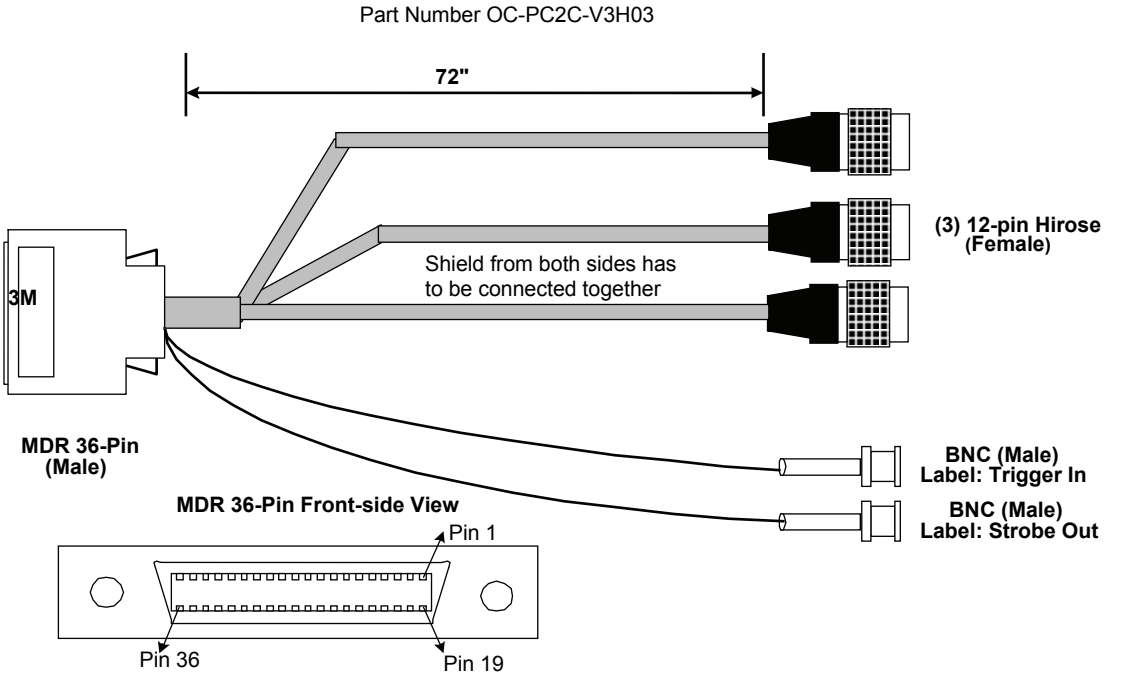


Figure 52: Interface cable

Hirose Cable 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
2	HS1	9	Coax 1 Wire
4	Digital GND	5	Coax 1 Shield
20	VS1	7	Coax 2 Wire
22	Digital GND	8	Coax 2 Shield
1	Video 1	4	Coax 3 Wire
19	Analog GND	3	Coax 3 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
3	V init/Camera Trig. 1	6	Coax 4 Wire
22	Digital GND	5	Coax 4 Shield
Hirose Cable 2			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
6	HS2	9	Coax 1 Wire

16	Digital GND	5	Coax 1 Shield
24	VS2	7	Coax 2 Wire
29	Digital GND	8	Coax 2 Shield
5	Video 2	4	Coax 3 Wire
23	Analog GND	3	Coax 3 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
7	V init/Camera Trig. 2	6	Coax 4 Wire
29	Digital GND	5	Coax 4 Shield
Hirose Cable 3			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
9	HS3	9	Coax 1 Wire
12	Digital GND	5	Coax 1 Shield
27	VS3	7	Coax 2 Wire
12	Digital GND	8	Coax 2 Shield
8	Video 3	4	Coax 3 Wire
26	Analog GND	3	Coax 3 Shield
32	+12V	2	Wire
33	+12V GND	1	Wire
10	V init/Camera Trig. 3	6	Coax 4 Wire
16	Digital GND	5	Coax 4 Shield
Separate Coax Cables			
Pin #	MDR 36-Pin (Male) Frame Grabber	BNC (Male) Connector Trigger In	
18	Ext_Trig1+	Coax Wire	
17	Ext_Trig1-	Coax Shield	
Pin #	MDR 36-Pin (Male) Frame Grabber	BNC (Male) Connector Strobe	
11	Strobe1	Coax Wire	
12	Digital GND	Coax Shield	

Cable 12: JAI CV-M Cameras (Pixel Clock and WEN pulse)

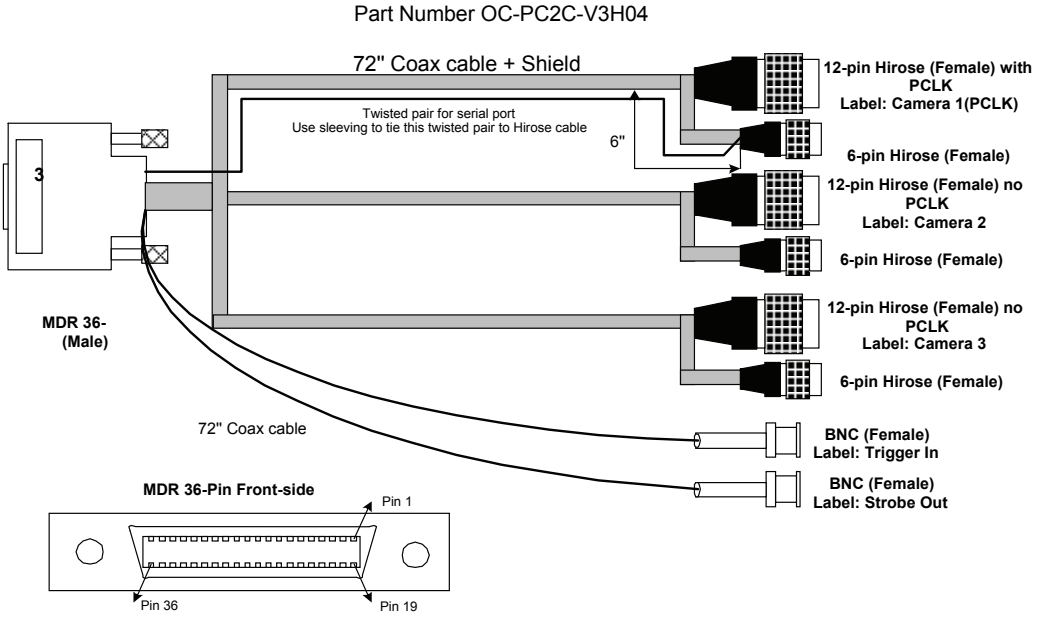


Figure 53: JAI CV-M camera cable

Note: A "coax" appellation following by a number (for example, coax 1) identifies which coax cable within the Hirose cable is used for a specific connection.

A "twisted pair" appellation refers to a separate cable used to supplement the twelve conductors on the Hirose cable. This cable must use sleeving to attach it to the corresponding Hirose cable.

Camera 1			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
1	Video1	4	Coax 1 Wire
19	Video1 AGND	3	Coax 1 Shield
2	HS1	6	Coax 2 Wire
4	Digital GND	5	Coax 2 Shield
20	VS1	7	Coax 3 Wire
4	Digital GND	12	Coax 3 Shield
36	Pixel Clock	9	Coax 4 Wire
29	Digital GND	8	Coax 4 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 6-Pin (Female)
3	Camera trigger 1	5	Wire
34	RX1	1	Twisted pair conductor 1
35	TX1	2	Twisted pair conductor 2
21	WEN1 (Write Enable) Out	6	Wire
Camera 2			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)
5	Video2	4	Coax 1 Wire
23	Video2 AGND	3	Coax 1 Shield
6	HS2	6	Coax 2 Wire
22	Digital GND	5	Coax 2 Shield
24	VS2	7	Coax 3 Wire
22	Digital GND	12	Coax 3 Shield
32	+12V	2	Wire
33	+12V GND	1	Wire
7	Camera trigger2	5	Coax 4 Wire
22	Digital GND	3	Coax 4 Shield
25	WEN2 (Write enable) Out	6	Wire
Camera 3			
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	Hirose 12-Pin (Female)

8	Video3	4	Coax 1 Wire
26	Video3 AGND	3	Coax 1 Shield
9	HS3	6	Coax 2 Wire
29	Digital GND	5	Coax 2 Shield
27	VS3	7	Coax 3 Wire
29	Digital GND	12	Coax 3 Shield
30	+12V	2	Wire
31	+12V GND	1	Wire
10	Camera trigger3	5	Coax 4 Wire
29	Digital GND	3	Coax 4 Shield
28	WEN3 (Write Enable) Out	6	Wire
BNC			
Pin #	**MDR 36-Pin (Male) Frame Grabber**	**Pin #**	**BNC (Male) Connector Trigger In**
18	Ext_Trig1+		Coax Wire
17	Ext_Trig1-		Coax Shield
Pin #	MDR 36-Pin (Male) Frame Grabber	Pin #	BNC (Male) Connector Strobe Out
11	Strobe1		Coax Wire
12	Digital GND		Coax Shield

Recommendation: It is recommended to use a 3M 10336-52F0-008 MDR36 shell or a 3M 10336-A200-00 MDR36 metal shell when constructing a cable connecting the PC2-Vision and camera. These shells use a quick release latch mechanism. Contact the 3M web page [http://www.3m.com/] for further information.

Sapera LT

Sapera Server and Parameters

The following table lists the Sapera Server available for PC2-Vision. Note that a single server supports both monochrome and RGB cameras.

Servers		Resources			
Name	**Description**	**Type**	**Name**	**Index**	**Description**
PC2-Vision_1	PC2-Vision	Acquisition	Mono 1	0	First monochrome video channel
			Mono 2	1	Second monochrome video channel
			Mono 3	2	Third monochrome video channel
			Mono 4	3	Fourth monochrome video channel
			Mono 5	4	Fifth monochrome video channel
			Mono 6	5	Sixth monochrome video channel
			RGB 1	0	First RGB video channel (J1)
			RGB 2	1	Second RGB video channel (J2)

The following tables describe the Sapera parameters and values supported by PC2-Vision. Refer to *Sapera Acquisition Parameters Reference* manual for a thorough description of each parameter.

CAMERA PARAMETERS	Values
CORACQ_PRM_CAM_NAME	Default Area Scan
CORACQ_PRM_CAM_RESET_DURATION	min = 1 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_RESET_METHOD	CORACQ_VAL_CAM_RESET_METHOD_1 (0x1)
CORACQ_PRM_CAM_RESET_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MAX	65535000 µs
CORACQ_PRM_CAM_TIME_INTEGRATE_DURATION_MIN	1 µs
CORACQ_PRM_CAM_TRIGGER_DURATION	min = 1 µs max = 65535000 µs step = 1 µs

CORACQ_PRM_CAM_TRIGGER_METHOD	CORACQ_VAL_CAM_TRIGGER_METHOD_1 (0x1)
CORACQ_PRM_CAM_TRIGGER_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_CHANNEL	CORACQ_VAL_CHANNEL_SINGLE (0x1)
CORACQ_PRM_CHANNELS_ORDER	CORACQ_VAL_CHANNELS_ORDER_NORMAL (0x1)
CORACQ_PRM_COUPLING	CORACQ_VAL_COUPLING_AC (0x1)
CORACQ_PRM_DETECT_HACTIVE	Not available
CORACQ_PRM_DETECT_PIXEL_CLK	Not available
CORACQ_PRM_DETECT_VACTIVE	Not available
CORACQ_PRM_FIELD_ORDER	CORACQ_VAL_FIELD_ORDER_ODD_EVEN (0x1) CORACQ_VAL_FIELD_ORDER_EVEN_ODD (0x2) CORACQ_VAL_FIELD_ORDER_NEXT_FIELD (0x4)
CORACQ_PRM_FRAME	CORACQ_VAL_FRAME_INTERLACE (0x1) CORACQ_VAL_FRAME_PROGRESSIVE (0x2)
CORACQ_PRM_FRAME_INTEGRATE_METHOD	Not available
CORACQ_PRM_FRAME_INTEGRATE_POLARITY	Not available
CORACQ_PRM_HACTIVE	min = 4 pixels max = 2048 pixels step = 4 pixels
CORACQ_PRM_HBACK_PORCH	min = 0 pixel max = 2044 pixels step = 1 pixel
CORACQ_PRM_HFRONT_PORCH	min = 0 pixel max = 2044 pixel step = 1 pixel
CORACQ_PRM_HSYNC	min = 1 pixel max = 2044 pixels step = 1 pixel
CORACQ_PRM_HSYNC_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_INTERFACE	CORACQ_VAL_INTERFACE_ANALOG (0x1)
CORACQ_PRM_PIXEL_CLK_11	12270000 Hz
CORACQ_PRM_PIXEL_CLK_DETECTION	CORACQ_VAL_RISING_EDGE (0x4)
CORACQ_PRM_PIXEL_CLK_EXT	min = 7000000 Hz max = 40000000 Hz step = 1 Hz
CORACQ_PRM_PIXEL_CLK_INT	min = 7000000 Hz max = 40000000 Hz step = 1 Hz
CORACQ_PRM_PIXEL_CLK_SRC	CORACQ_VAL_PIXEL_CLK_SRC_INT (0x1) CORACQ_VAL_PIXEL_CLK_SRC_EXT (0x2)
CORACQ_PRM_PIXEL_DEPTH	8 bits
CORACQ_PRM_SCAN	CORACQ_VAL_SCAN_AREA (0x1)
CORACQ_PRM_SIGNAL	CORACQ_VAL_SIGNAL_SINGLE_ENDED (0x1)

CORACQ_PRM_SYNC	CORACQ_VAL_SYNC_COMP_VIDEO (0x1) CORACQ_VAL_SYNC_COMP_SYNC (0x2) CORACQ_VAL_SYNC_SEP_SYNC (0x4) CORACQ_VAL_SYNC_INT_SYNC (0x8) CORACQ_VAL_SYNC_RED (0x10) CORACQ_VAL_SYNC_GREEN (0x20) CORACQ_VAL_SYNC_BLUE (0x40)
CORACQ_PRM_TAP_1_DIRECTION	CORACQ_VAL_TAP_DIRECTION_LR (0x1) CORACQ_VAL_TAP_DIRECTION_UD (0x4) CORACQ_VAL_TAP_DIRECTION_FROM_TOP (0x10)
CORACQ_PRM_TAP_OUTPUT	CORACQ_VAL_TAP_OUTPUT_SEGMENTED (0x2)
CORACQ_PRM_TAPS	min = 1 tap max = 1 tap step = 1 tap
CORACQ_PRM_TIME_INTEGRATE_METHOD	CORACQ_VAL_TIME_INTEGRATE_METHOD_1 (0x1) CORACQ_VAL_TIME_INTEGRATE_METHOD_2 (0x2) CORACQ_VAL_TIME_INTEGRATE_METHOD_3 (0x4) CORACQ_VAL_TIME_INTEGRATE_METHOD_4 (0x8) CORACQ_VAL_TIME_INTEGRATE_METHOD_5 (0x10) CORACQ_VAL_TIME_INTEGRATE_METHOD_6 (0x20) CORACQ_VAL_TIME_INTEGRATE_METHOD_7 (0x40)
CORACQ_PRM_TIME_INTEGRATE_PULSE0_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE0_DURATION	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE0_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_DURATION	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_PULSE1_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_VACTIVE	min = 1 line max = 2048 lines step = 1 line
CORACQ_PRM_VBACK_INVALID	min = 0 line max = 100 lines step = 1 line

CORACQ_PRM_VBACK_PORCH	min = 0 line max = 2047 lines step = 1 line
CORACQ_PRM_VFRONT_PORCH	min = 0 line max = 2047 lines step = 1 line
CORACQ_PRM_VIDEO	CORACQ_VAL_VIDEO_MONO (0x1) CORACQ_VAL_VIDEO_RGB (0x8)
CORACQ_PRM_VIDEO_LEVEL_MAX	Default = 0 µV
CORACQ_PRM_VIDEO_LEVEL_MIN	Default = 0 µV
CORACQ_PRM_VIDEO_STD	CORACQ_VAL_VIDEO_STD_NON_STD (0x1) CORACQ_VAL_VIDEO_STD_RS170_NTSC (0x2) CORACQ_VAL_VIDEO_STD_CCIR_PAL (0x4)
CORACQ_PRM_VSYNC	min = 1 line max = 2047 lines step = 1 line
CORACQ_PRM_VSYNC_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_WEN_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)

VIC PARAMETERS	**Values**
CORACQ_PRM_BIT_ORDERING	CORACQ_VAL_BIT_ORDERING_STD (0x1)
CORACQ_PRM_BRIGHTNESS	min = -20000 (1/1000 %) max = 29000 (1/1000 %) step = 196 (1/1000 %)
CORACQ_PRM_BRIGHTNESS_BLUE	min = -20000 (1/1000 %) max = 29000 (1/1000 %) step = 196 (1/1000 %)
CORACQ_PRM_BRIGHTNESS_GREEN	min = -20000 (1/1000 %) max = 29000 (1/1000 %) step = 196 (1/1000 %)
CORACQ_PRM_BRIGHTNESS_RED	min = -20000 (1/1000 %) max = 29000 (1/1000 %) step = 196 (1/1000 %)
CORACQ_PRM_CAM_RESET_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_RESET_ENABLE	TRUE FALSE
CORACQ_PRM_CAM_TRIGGER_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_CAM_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_CAMSEL	CAMSEL_MONO = from 0 to 5

	CAMSEL_COLOR not available CAMSEL_YC not available CAMSEL_RGB = from 0 to 1
CORACQ_PRM_CONTRAST	min = 60000 (1/1000 %) max = 170000 (1/1000 %) step = 1000 (1/1000 %)
CORACQ_PRM_CONTRAST_BLUE	min = 60000 (1/1000 %) max = 170000 (1/1000 %) step = 1000 (1/1000 %)
CORACQ_PRM_CONTRAST_GREEN	min = 60000 (1/1000 %) max = 170000 (1/1000 %) step = 1000 (1/1000 %)
CORACQ_PRM_CONTRAST_RED	min = 60000 (1/1000 %) max = 170000 (1/1000 %) step = 1000 (1/1000 %)
CORACQ_PRM_CROP_HEIGHT	min = 1 line max = 2048 lines step = 1 line
CORACQ_PRM_CROP_LEFT	min = 0 pixel max = 2044 pixels step = 1 pixel
CORACQ_PRM_CROP_TOP	min = 0 line max = 2047 lines step = 1 line
CORACQ_PRM_CROP_WIDTH	min = 4 pixels max = 2048 pixels step = 4 pixels
CORACQ_PRM_DC_REST_MODE	CORACQ_VAL_DC_REST_MODE_AUTO (0x1) CORACQ_VAL_DC_REST_MODE_ON (0x2) CORACQ_VAL_DC_REST_MODE_OFF (0x4)
CORACQ_PRM_DC_REST_START	min = 0 pixel max = 2047 pixels step = 1 pixel
CORACQ_PRM_DC_REST_WIDTH	min = 0 pixel max = 2047 pixels step = 1 pixel
CORACQ_PRM_DECIMATE_COUNT	Default = 0
CORACQ_PRM_DECIMATE_METHOD	CORACQ_VAL_DECIMATE_DISABLE (0x1) CORACQ_VAL_DECIMATE_ODD (0x8) CORACQ_VAL_DECIMATE_EVEN (0x10)
CORACQ_PRM_EXT_TRIGGER_DETECTION	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2) CORACQ_VAL_RISING_EDGE (0x4) CORACQ_VAL_FALLING_EDGE (0x8)
CORACQ_PRM_EXT_TRIGGER_DURATION	min = 0 µs max = 255 µs step = 1 µs
CORACQ_PRM_EXT_TRIGGER_ENABLE	CORACQ_VAL_EXT_TRIGGER_OFF (0x1) CORACQ_VAL_EXT_TRIGGER_ON (0x8)

CORACQ_PRM_EXT_TRIGGER_FRAME_COUNT	Default = 1 frame
CORACQ_PRM_EXT_TRIGGER_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1) CORACQ_VAL_LEVEL_422 (0x2)
CORACQ_PRM_EXT_TRIGGER_SOURCE	0: automatic selection 1: first MDR-36 (J1) 2: second MDR-36 (J2)
CORACQ_PRM_FIX_FILTER_ENABLE	TRUE FALSE
CORACQ_PRM_FIX_FILTER_SELECTOR	0: 6 MHz 1: 12 MHz
CORACQ_PRM_FLIP	Not available
CORACQ_PRM_FRAME_INTEGRATE_COUNT	Not available
CORACQ_PRM_FRAME_INTEGRATE_ENABLE	Not available
CORACQ_PRM_FRAME_LENGTH	CORACQ_VAL_FRAME_LENGTH_FIX (0x1)
CORACQ_PRM_HSYNC_REF	CORACQ_VAL_SYNC_REF_BEGIN (0x1)
CORACQ_PRM_HUE	Not available
CORACQ_PRM_INT_FRAME_TRIGGER_ENABLE	TRUE FALSE
CORACQ_PRM_INT_FRAME_TRIGGER_FREQ	min = 1 milli-Hz max = 1000000000 milli-Hz step = 1 milli-Hz
CORACQ_PRM_LUT_ENABLE	TRUE FALSE
CORACQ_PRM_LUT_FORMAT	Default = CORACQ_VAL_OUTPUT_FORMAT_MONO8
CORACQ_PRM_LUT_MAX	1
CORACQ_PRM_LUT_NENTRIES	256 entries
CORACQ_PRM_LUT_NUMBER	Default = 0
CORACQ_PRM_MASTER_MODE	CORACQ_VAL_MASTER_MODE_DISABLE (0x0) CORACQ_VAL_MASTER_MODE_HSYNC_VSYNC (0x1) CORACQ_VAL_MASTER_MODE_HSYNC (0x2) CORACQ_VAL_MASTER_MODE_VSYNC (0x4)
CORACQ_PRM_MASTER_MODE_HSYNC_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_MASTER_MODE_VSYNC_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_OUTPUT_FORMAT	CORACQ_VAL_OUTPUT_FORMAT_MONO8 CORACQ_VAL_OUTPUT_FORMAT_RGB8888
CORACQ_PRM_PIXEL_MASK	Not available
CORACQ_PRM_PLANAR_INPUT_SOURCES	Bitflag where each bit (from to 5) represent the corresponding camera index 0x00: disabled 0x03: CAM1 and CAM2 0x07: CAM1, CAM2 and CAM3 0x18: CAM4 and CAM5

	0x38: CAM4, CAM5 and CAM6
CORACQ_PRM_PROG_FILTER_ENABLE	Not available
CORACQ_PRM_PROG_FILTER_FREQ	Not available
CORACQ_PRM_SATURATION	Not available
CORACQ_PRM_SCALE_HORZ	min = 4 pixels/line max = 2048 pixels/line step = 4 pixels/line
CORACQ_PRM_SCALE_HORZ_METHOD	CORACQ_VAL_SCALE_METHOD_DISABLE (0x1) CORACQ_VAL_SCALE_METHOD_POW2 (0x8)
CORACQ_PRM_SCALE_VERT	min = 1 lines/frame max = 2048 lines/frame step = 1 lines/frame
CORACQ_PRM_SCALE_VERT_METHOD	CORACQ_VAL_SCALE_METHOD_DISABLE (0x1) CORACQ_VAL_SCALE_METHOD_POW2 (0x8)
CORACQ_PRM_SHARED_CAM_RESET	Not available
CORACQ_PRM_SHARED_CAM_TRIGGER	Not available
CORACQ_PRM_SHARED_EXT_TRIGGER	Not available
CORACQ_PRM_SHARED_FRAME_INTEGRATE	Not available
CORACQ_PRM_SHARED_STROBE	Not available
CORACQ_PRM_SHARED_TIME_INTEGRATE	Not available
CORACQ_PRM_SHARPNESS	min = 0 max = 0 step = 1
CORACQ_PRM_SNAP_COUNT	Default = 1 frame
CORACQ_PRM_STROBE_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_STROBE_DELAY_2	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_STROBE_DURATION	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_STROBE_ENABLE	TRUE FALSE
CORACQ_PRM_STROBE_LEVEL	CORACQ_VAL_LEVEL_TTL (0x1)
CORACQ_PRM_STROBE_METHOD	CORACQ_VAL_STROBE_METHOD_1 (0x1) CORACQ_VAL_STROBE_METHOD_2 (0x2) CORACQ_VAL_STROBE_METHOD_4 (0x8)
CORACQ_PRM_STROBE_POLARITY	CORACQ_VAL_ACTIVE_LOW (0x1) CORACQ_VAL_ACTIVE_HIGH (0x2)
CORACQ_PRM_TIME_INTEGRATE_DELAY	min = 0 µs max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_DURATION	min = 0 µs

	max = 65535000 µs step = 1 µs
CORACQ_PRM_TIME_INTEGRATE_ENABLE	TRUE FALSE
CORACQ_PRM_VIC_NAME	Default Area Scan
CORACQ_PRM_VSYNC_REF	CORACQ_VAL_SYNC_REF_BEGIN (0x1)
CORACQ_PRM_VSYNC_TIMEOUT	Not available
CORACQ_PRM_WEN_ENABLE	TRUE FALSE

ACQUISITION PARAMETERS	**Values**
CORACQ_PRM_EVENT_TYPE	CORACQ_VAL_EVENT_TYPE_START_OF_FIELD (0x10000) CORACQ_VAL_EVENT_TYPE_START_OF_ODD (0x20000) CORACQ_VAL_EVENT_TYPE_START_OF_EVEN (0x40000) CORACQ_VAL_EVENT_TYPE_START_OF_FRAME (0x80000) CORACQ_VAL_EVENT_TYPE_END_OF_FIELD (0x100000) CORACQ_VAL_EVENT_TYPE_END_OF_ODD (0x200000) CORACQ_VAL_EVENT_TYPE_END_OF_EVEN (0x400000) CORACQ_VAL_EVENT_TYPE_END_OF_FRAME (0x800000) CORACQ_VAL_EVENT_TYPE_EXTERNAL_TRIGGER (0x1000000) CORACQ_VAL_EVENT_TYPE_VERTICAL_SYNC (0x2000000)
CORACQ_PRM_LABEL	Analog Interface
CORACQ_PRM_SIGNAL_STATUS	CORACQ_VAL_SIGNAL_HSYNC_PRESENT (0x1) CORACQ_VAL_SIGNAL_HSYNC_LOCK (0x10)

TRANSFER PARAMETERS	**Values**
CORXFER_PRM_EVENT_TYPE	CORXFER_VAL_EVENT_TYPE_END_OF_FRAME (0x00800000) CORXFER_VAL_EVENT_TYPE_END_OF_FIELD (0x00100000) CORXFER_VAL_EVENT_TYPE_END_OF_TRANSFER (0x04000000)

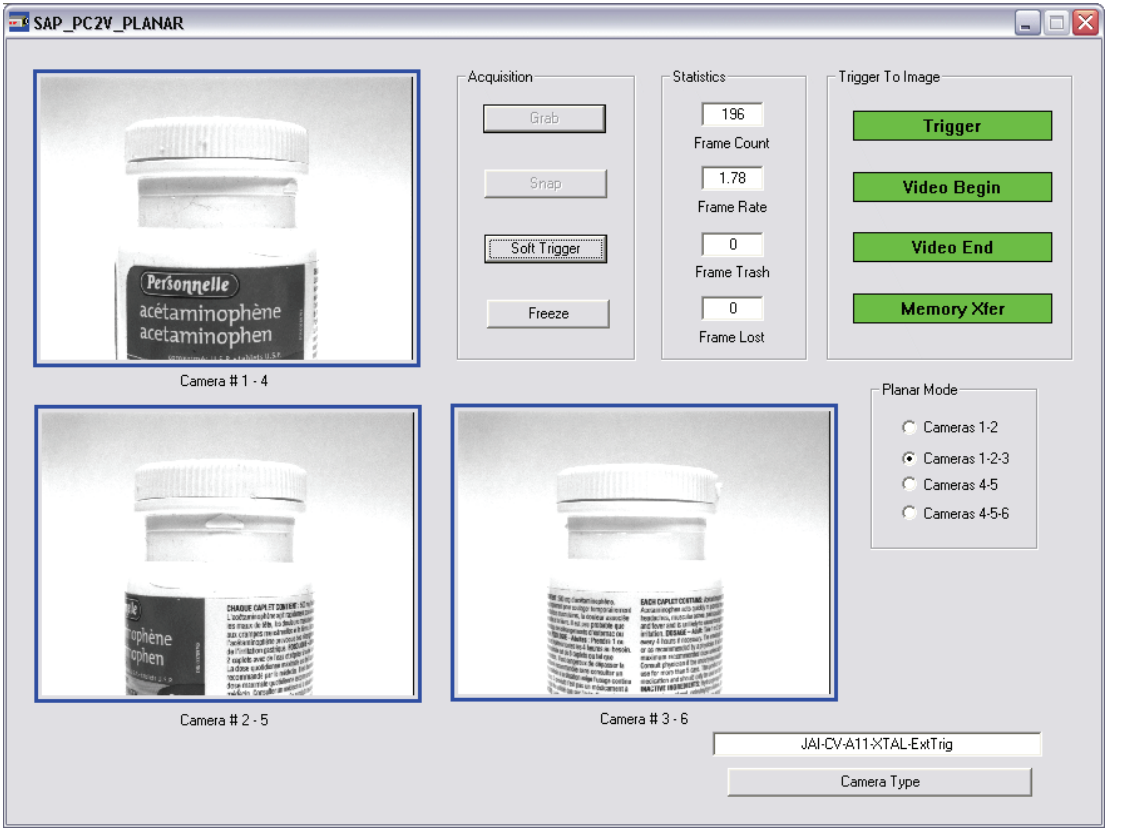
PC2-Vision Specific Sapera Examples

PC2-Vision Sapera driver installation package comes with the following example programs for PC2-Vision. Full source code is included. You need Microsoft Visual C++ 6.0 or later to recompile the examples.

SAP_PC2V_Planar	Simultaneous acquisition and display of three genlocked cameras
SAP_PC2V_ManualCamSwitch	Manual camera switching from up to six monochrome cameras
SAP_PC2V_Parallel_IO	Parallel I/O access techniques

SAP_PC2V_Planar

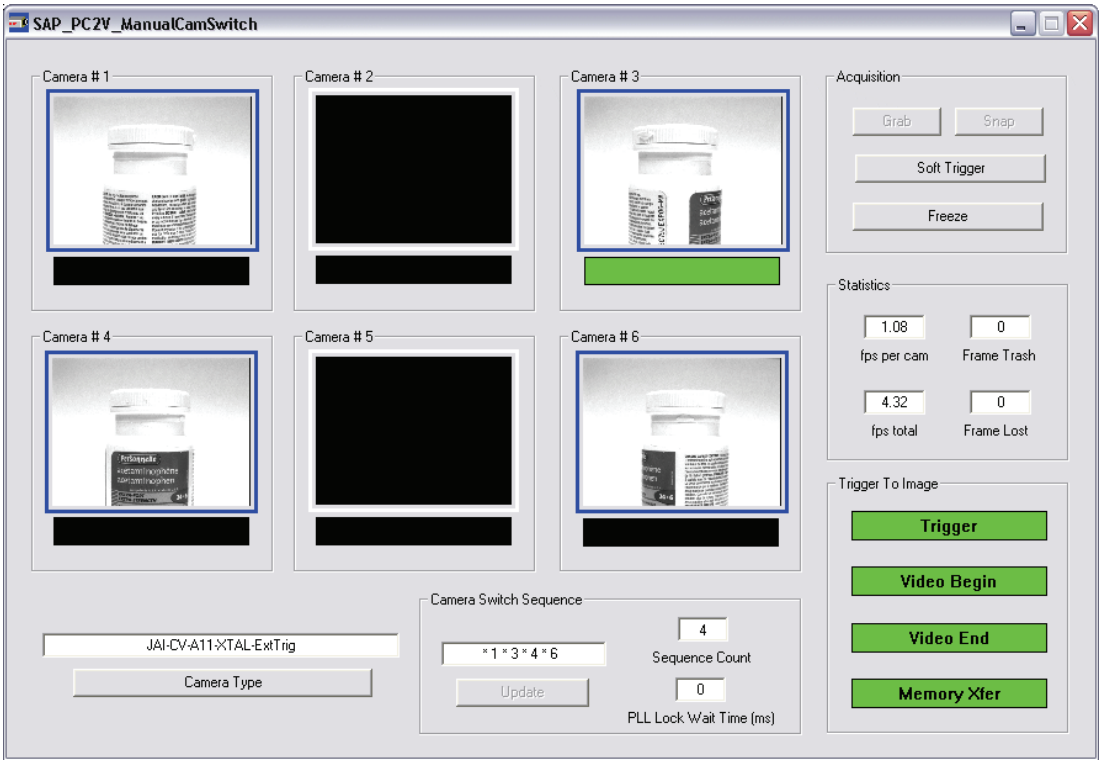
Title	**Acquisition from three genlocked cameras**
Description	Simultaneous acquisition and display of three genlocked cameras in Planar transfer mode
Features	- 3 independent displays - Camera and port selection - Grab or snap - SW trigger - Statistics indicators - Frame Trash count for host buffer memory management - Frame Lost count for PCI bandwidth problems - Trigger-to-image indicators
Setup	- 3 genlockable monochrome cameras (must accept external VD and HD signals) - Camera cable supporting three monochrome cameras - 1 PC2-Vision
Project location	**Installation Directory\PC2-Vision\Demos\SAP_PC2V_Planar**



SAP_PC2V_ManualCamSwitch

Title	Manual camera switching, one camera at a time
Description	Camera switching between (and up to) six cameras. Camera can be in PLL mode or genlocked.
Features	- 6 independent displays - Camera and switching sequence selection - Grab or snap - SW trigger - Statistics indicators - Frame Trash count for host buffer memory management - Frame Lost count for PCI bandwidth problems - PLL Lock wait time parameter to compensate for PLL lock delay. - Trigger-to-image indicators

Setup	- From 1 to 6 genlocked cameras - 1 or 2 camera cables - 1 PC2-Vision
Project location	**Installation Directory\PC2-Vision\Demos\SAP_PC2V_ManualCamSwitch**



SAP_PC2V_Parallel_IO

Title	Parallel I/O port access
Description	Shows how to use the PC2-Vision's Parallel I/O port.
Features	- States indicator for each input and output pin - Parallel I/O interrupt support
Setup	- Cable for Parallel I/O port - 1 PC2-Vision
Project location	**Installation Directory\PC2-Vision\Demos\SAP_PC2V_Parallel_IO**

Sapera Software Example

Grab Demo Overview

Program	**Start•Programs•Sapera LT•Demos•Grab Demo**
Program file	**\DALSA\Sapera\Demos\Classes\vc\GrabDemo\Release\GrabDemo.exe**
Workspace	**\DALSA\Sapera\Demos\Classes\vc\SapDemos.dsw**
Description	This program demonstrates the basic acquisition functions included in the Sapera library. The program allows you to acquire images, either in continuous or in one-shot mode, while adjusting acquisition parameters. The program code can be extracted for use within your own application.
Remarks	Grab Demo was built using Visual C++ 6.0 by means of the MFC library and is based on the Sapera standard API and Sapera C++ classes. See the Sapera User's and Reference manuals for further information.

Using the Grab Demo

Server Selection

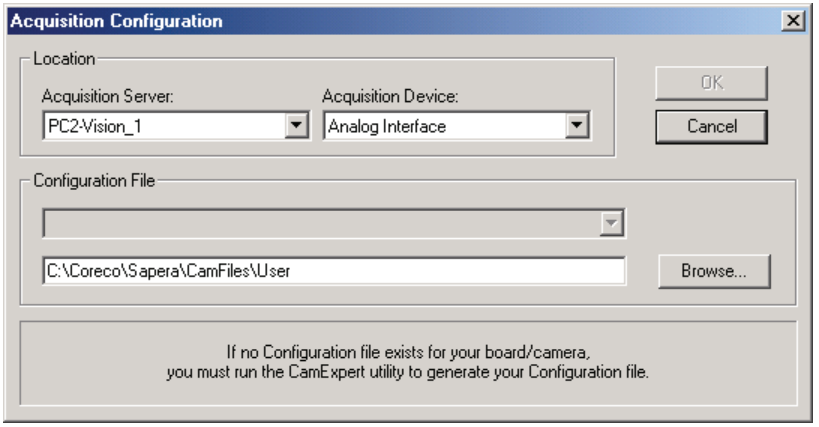
Run Grab Demo from the Start Menu: **Start•All Programs•DALSA•Sapera LT•Demos•Frame Grabbers•Grab Demo**.

When activated, Grab Demo first displays the "Acquisition Configuration" window. The first drop down menu allows you to select any installed Sapera acquisition server (that is, installed DALSA acquisition hardware using Sapera drivers). The second drop down menu allows you to select the available input devices present on the selected server.

CCF File Selection

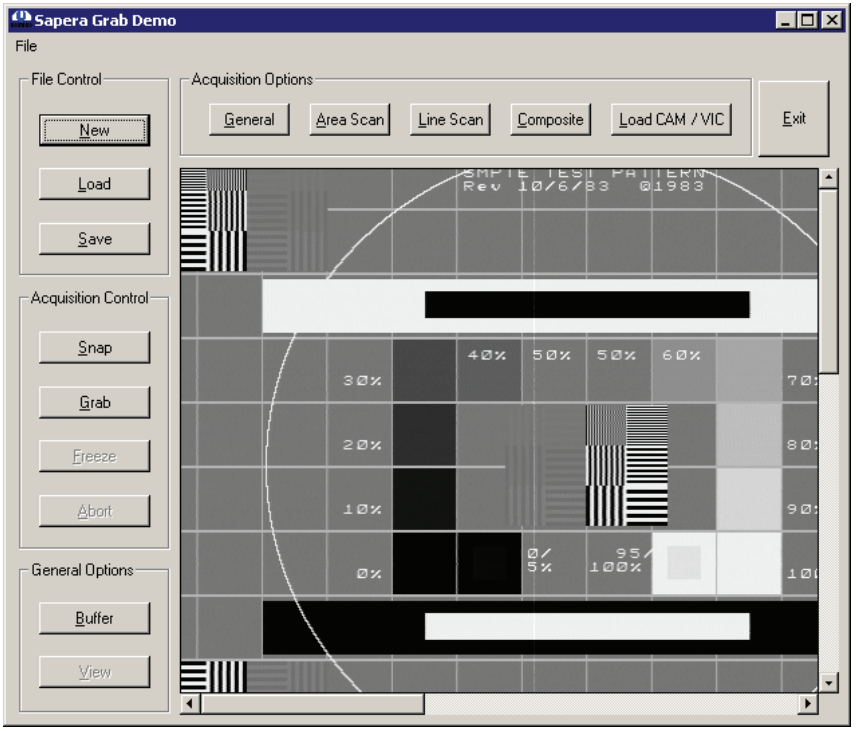
The "Acquisition Configuration" window is also used to select the camera configuration file required for the connected camera. Sapera camera files contain timing parameters and video conditioning parameters. The default folder used for camera configuration files is also used by the CamExpert utility to save user generated or modified camera files.

Use Sapera CamExpert to generate the camera configuration file based on the timing and control parameters entered. The CamExpert live acquisition window allows immediate verification of the parameters. CamExpert reads both Sapera *.cca and *.cvi files for backwards compatibility with the original Sapera camera files.



Grab Demo Main Window

The main window provides control buttons and a central region where the grabbed image is displayed. Developers can use the source code supplied with the demo as a foundation to quickly create and test the desired imaging application.



The various functions are described below:

File Control

Three controls are provided for image file transfers

- **New:** Clears the current image frame buffer.
- **Load:** Retrieves images in BMP, TIF, CRC, JPG, and RAW formats.
- **Save:** Prompts for a file name, file save location, and image format.

Acquisition Options

Note that unsupported functions are grayed out and not selectable. Function support is dependent on the frame grabber hardware in use.

- **General – Acquisition Settings:** Allows for PC2-Vision external trigger mode enabling.
- **Area Scan – Camera Control:** Provides trigger, reset, and integrate controls when supported by the current hardware and driver. Also offers master HS and VS output.
- **Line Scan – Camera Control:** This dialog is not applicable to the PC2-Vision.
- **Composite - Conditioning:** Offers Brightness and Contrast controls.
- **Load CAM/VIC:** Opens the dialog window Acquisition Parameters allowing the user to load a new set of camera files. This is the same window displayed when the Sapera Acquisition Demo is first started.

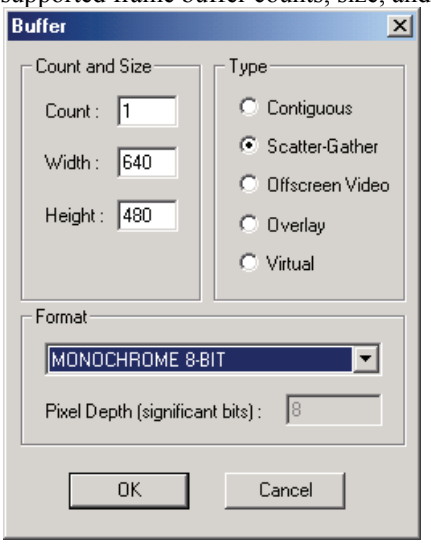
Acquisition Control

- **Grab:** Displays live digitized video from your video source. If your source is a camera, focus and adjust the lens aperture for the best exposure. Use a video generator as a video source to acquire reference images.
- **Freeze:** Stops live grab mode. The grabbed image can be saved to disk via the **File Control•Save** control.
- **Snap:** A single video frame is grabbed.
- **Abort** Exits the current grab process immediately. If any video signal problem prevents the freeze function from ending the grab, click **Abort**.

General Options

Note: functions grayed out are not supported by acquisition hardware.

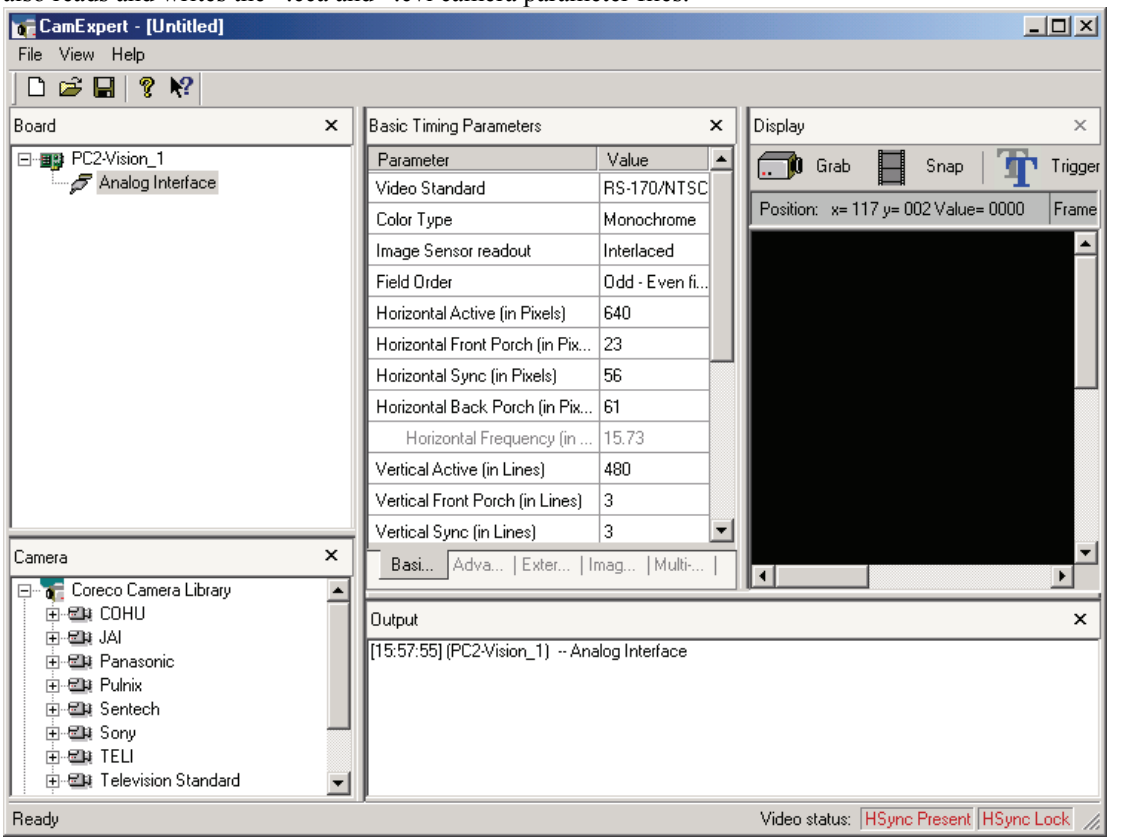
- **Buffer:** Select from supported frame buffer counts, size, and types.



- **Count and Size**: Select the number of frame buffers and the image size here.
- Type – **Contiguous**: Frame buffers are allocated in contiguous system memory (single memory block - no segmentation).
- Type – **Scatter-Gather**: Frame buffers are allocated throughout system memory in noncontiguous memory (paged pool). Pages are locked in physical memory so a scatter-gather list can be constructed. This type allows for the allocation of very large size buffers or large buffer counts.
- Type – **Off-screen Video**: The buffer is allocated in off-screen video memory and uses the display adapter hardware to perform a fast copy from video memory to video memory.
- Type – **Overlay**: The frame buffer is allocated in video memory where the display adapter overlay hardware uses color-keying to view the overlay buffer.
- **Format**: Shows frame buffer pixel formats as supported by the hardware and camera files used.

Using Sapera CamExpert with PC2-Vision

CamExpert is the camera interfacing tool for frame grabber boards supported by the Sapera library. CamExpert generates the Sapera camera configuration file (*yourcamera.ccf*) based on timing and control parameters entered. For backward compatibility with previous versions of Sapera, CamExpert also reads and writes the *.cca and *.cvi camera parameter files.



An important component of CamExpert is its live acquisition display window which allows immediate verification of timing or control parameters without the need to run a separate acquisition program.

For context sensitive help, click on the button then click on a camera configuration parameter. A short description of the configuration parameter will be shown in a popup. Click on the button to open the help file for more descriptive information on CamExpert.

The central section of CamExpert provides access to the various Sapera parameters of PC2-Vision. It is divided into five tabs.

Basic Timing Parameters	Basic parameters used to define the timing of the camera. This includes the vertical, horizontal, and pixel clock frequency. This tab is sufficient to configure a free-running camera.
Advanced Control Parameters	Advanced parameters used to configure camera control mode and strobe output. Also provides analog signal conditioning (brightness, contrast, DC restoration, etc.)
External Trigger Parameters	Parameters to configure the external trigger characteristics.
Image Buffer and AOI Parameters	Control of the host buffer dimension and format.
Multi-Camera Control Parameters	Provides camera selection. Includes planar transfer.

Camera Files Distributed with Sapera

The Sapera distribution CD-ROM includes camera files that are compatible to PC2-Vision supported cameras. When using the Sapera CamExpert program, you may use the camera files (CCA) provided to generate a camera configuration file (CCF) that describes the desired camera and frame grabber configuration.

TELEDYNE DALSA continually updates their camera application library that contains application information and prepared camera files. Along with the camera search utility on the DALSA web site, a number of camera files are ready to download from the DALSA FTP site [ftp://ftp.DALSA.com/public/Sapera/CamFile_Updates]. Camera files are ASCII text and can be read with Windows Notepad on any computer without having Sapera installed.

Overview of Sapera Acquisition Parameter Files (*.ccf or *.cca/*.cvi)

Concepts and Differences between the Parameter Files

There are two components to the legacy Sapera acquisition parameter file set: CCA files (also called cam files) and CVI files (also called VIC files, that is, video input conditioning). The files store video-signal parameters (CCA) and video conditioning parameters (CVI), which in turn simplifies programming the frame grabber acquisition hardware for the camera in use. **Sapera LT 5.10** introduces a new camera configuration file (**CCF**) that combines the CCA and CVI files into one file.

Typically, a camera application will use a CCF file per camera operating mode (or one CCA file in conjunction with several CVI files, where each CVI file defines a specific camera operating mode). An application can also have multiple CCA/CCF files so as to support different image format modes supported by the camera or sensor (such as image binning or variable ROI).

CCF File Details

Files using the ".CCF" extension (DALSA Camera Configuration file) are essentially the camera (CCA) and frame grabber (CVI) parameters grouped into one file for easier configuration file management. This is the default Camera Configuration file used with Sapera LT 5.10 and the CamExpert utility.

CCA File Details

TELEDYNE DALSA distributes camera files using the ".CCA" extension (DALSA CAMERA files) that contains all parameters describing the camera video signal characteristics and operation modes (that is, what the camera outputs). The Sapera parameter groups located within the file are:

- Video format and pixel definitions.
- Video resolution (pixel rate, pixels per line, and lines per frame).
- Synchronization source and timings.
- Channels/Taps configuration.
- Supported camera modes and related parameters.
- I/O hardware signal assignment.

CVI File Details

Legacy files using the ".CVI" extension (DALSA VIDEO files) contain all operating parameters related to the frame grabber board, that is, what the frame grabber can actually do with camera controls or incoming video. The Sapera parameter groups located within the file:

- Activates and sets any supported camera control mode or control variable.
- Defines the integration mode and duration.
- Defines the strobe output control.
- Allocates the frame grabber transfer ROI, the host video buffer size and buffer type (RGB888, RGB101010, MONO8, MONO16).
- Configuration of line/frame trigger parameters such as source (internal via the frame grabber /external via some outside event), electrical format (TTL, LVDS, OPTO-isolated), and signal active edge or level characterization.

Camera Interfacing Check List

Before undertaking the task of interfacing a camera from scratch using CamExpert:

- Confirm that TELEDYNE DALSA has not already published an application note with camera files (http://www.dalsa.com/mv).
- Confirm that Sapera does not already have a .cca file for your camera installed on your hard disk. If there is a .cca file supplied with Sapera, then use CamExpert to automatically generate the .ccf file with default parameter values matching the frame grabber capabilities.
- Check if the Sapera installation has a similar type of camera file. A similar .cca file can be loaded into CamExpert where it is modified to match timing and operating parameters for your camera and then save them as Camera Configuration files (.ccf), or as a new .cca & .cvi camera file pair for applications built with Sapera 4.2 or earlier.
- Finally, if your camera type has never been interfaced, run CamExpert after installing Sapera and the acquisition board driver, select the board acquisition server, and enter the camera parameters.

IFC

IFC Software Examples

IFC Examples for PC2-Vision

IFC installation package comes with the following example programs for PC2-Vision. Full source code is included. You need Microsoft Visual C++ 6.0 or later to recompile the examples.

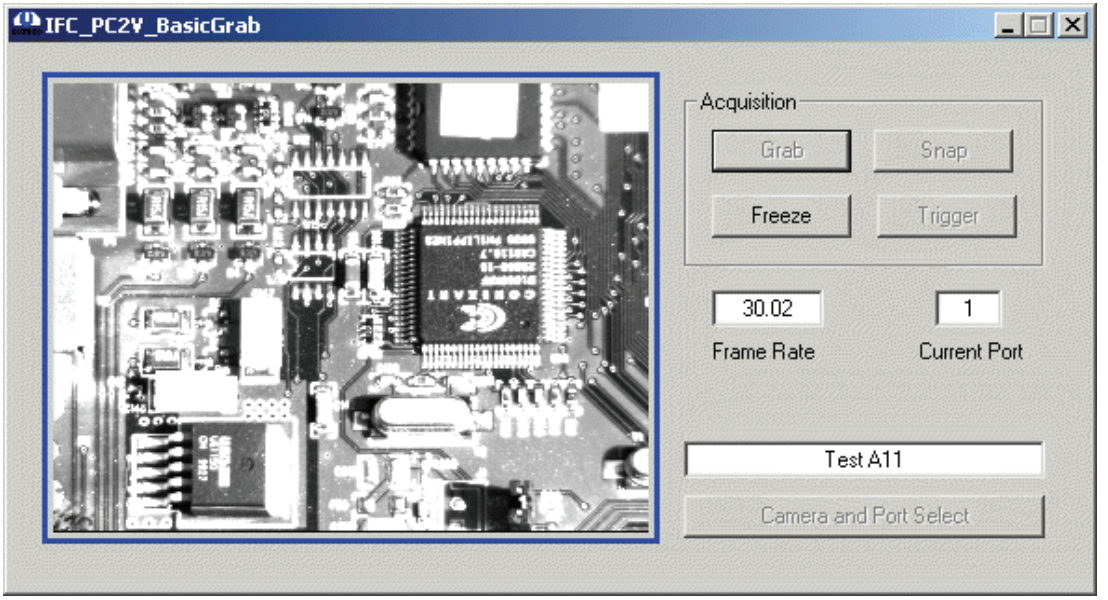
Examples are divided into five categories:

Basic Examples	
BasicGrab	Basic acquisition and display
BasicSoftOverlay	Basic acquisition and display along with text drawing in a software overlay
BasicHardOverlay	Basic acquisition and display in a hardware overlay
Parallel I/O	Demonstrates how to access the I/O pins present on the Parallel I/O connector
ThreadProc	Demonstrates how to do acquisition in host buffer and perform image processing
ThreadTrig	Triggers camera with an external trigger pulse
Camera Switching Examples	
6Cam-2Grab	Synchronized acquisition from 2 groups of 3 cameras using fast camera switching
CamSwitch	Dynamic switching between (and/or up to) 6 synchronized cameras
CamSwitch-Planar Vertical	Shows how to acquire and switch between 2 groups of 3 cameras with a single ring and a single buffer
Manual CamSwitch	Manual camera switching based on the Snap function call
Switcher	Fast camera switching from up to six synchronized cameras
Frame Delay Readout Examples	
FrameDelay	Demonstrates how to acquire six cameras (maximum) simultaneously
FrameDelayDlg	Dialog-box-based application demonstrating frame delay readout
FrameDelay-Planar Vertical	Shows how to acquire from 6 cameras in frame delay mode using the planar vertical mode

Miscellaneous Examples	
4Boards	Demonstrates how to acquire from up to 4 PC2-Vision boards
Interrupt	Demonstrates how to use interrupts available on PC2-Vision
PulseGen	Use Vixn to generate high-precision pulses on the Parallel I/O output
SeqSnap	Snaps a small number of images into host memory and replays them
Vixn	Shows how to use Vixn and explains why the response is fast and steady
Planar Transfer Examples	
3Cameras	Simultaneous acquisition and display of three synchronized cameras (dialog-box application)
3Cam-Planar Vertical	Shows how to acquire from 3 cameras with a single ring and a single buffer
3Cams-1Grab	Acquisition from 3 synchronized cameras (MDI application)
3Cams-1Ring	Simultaneous acquisition and display of three genlocked cameras in planar mode in a single ring of acquisition buffers
Grab3	Simultaneous acquisition from 3 monochrome cameras with live display

IFC_PC2V_BasicGrab

Title	Basic grabbing
Description	Basic acquisition and display with an Image Server. Memory allocation not required.
Features	- Dialog-box-based application - Camera and port selection - Grab or snap - SW trigger - Frame rate indicator
Setup	- Any RS-170 or CCIR camera - Camera cable - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_BasicGrab**



IFC_PC2V_BasicSoftOverlay

Title	Basic software overlay
Description	Basic acquisition and display with text drawing in a software overlay. The software overlay allows you to draw over your live image using the Windows GDI. It is not in the video memory and it is not as fast as a hardware overlay.
Features	- Dialog-box-based application - Camera and port selection - Grab or snap - SW trigger - Frame rate indicator
Setup	- Any RS-170 or CCIR camera - Camera cable - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_BasicSoftOverlay**

IFC_PC2V_BasicHardOverlay

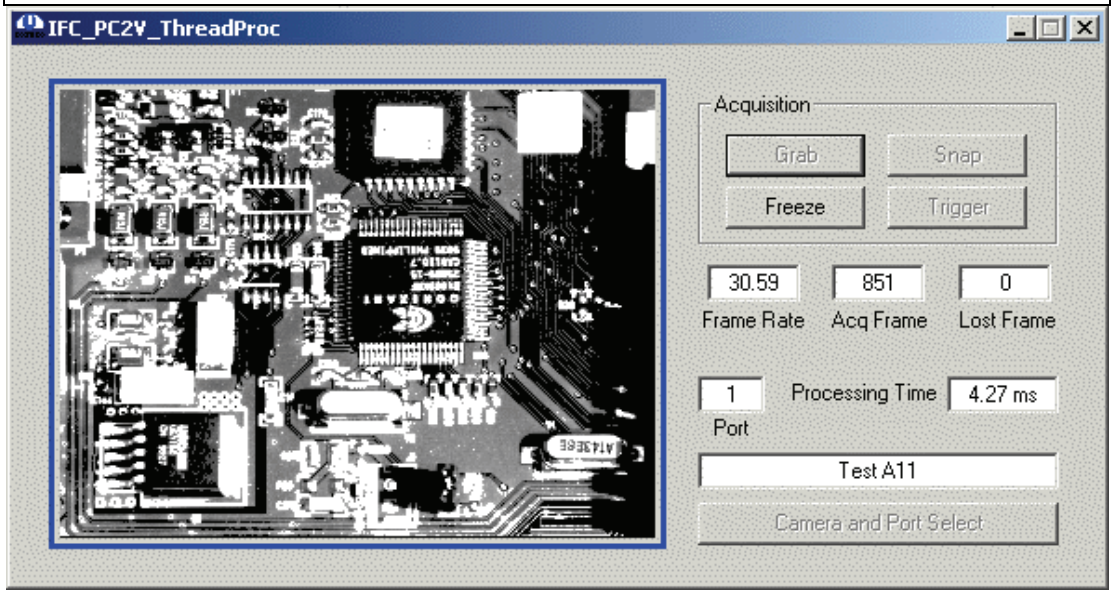
Title	Basic hardware overlay
Description	Basic acquisition and display in a hardware overlay with text drawing in the standard graphic surface. The hardware overlay is physically in the video memory of your display controller and converts in real-time, pixels in Y-Cr-Cb color format to the R-G-B format of your monitor. It also takes care of the scaling in real-time (zoom). The benefit of using a hardware overlay is an extremely fast live display because the host CPU does not have to do the pixel conversion and the image scaling. Keep in mind that the live image is in the overlay and the drawn text is in the standard graphic surface. The overlay, and hence the live image, is visible only if you draw the keying color in the standard graphic surface over the overlay.
Features	- Dialog-box-based application - Camera and port selection - Grab or snap - SW trigger - Frame rate indicator
Setup	- Any RS-170 or CCIR camera - Camera cable - 1 PC2-Vision - Display Controller with a hardware overlay
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_BasicHardOverlay**

IFC_PC2V_Parallel_IO

Title	Parallel Input/Output Connector
Description	Access to all I/O pins of the Parallel I/O connector
Features	- Dialog-box-based application -8 general inputs -8 general outputs -Control of strobe pins -Interrupt pin
Setup	-1 PC2-Vision -Connector on the Parallel I/O 26-pin header
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_Parallel_IO**

IFC_PC2V_ThreadProc

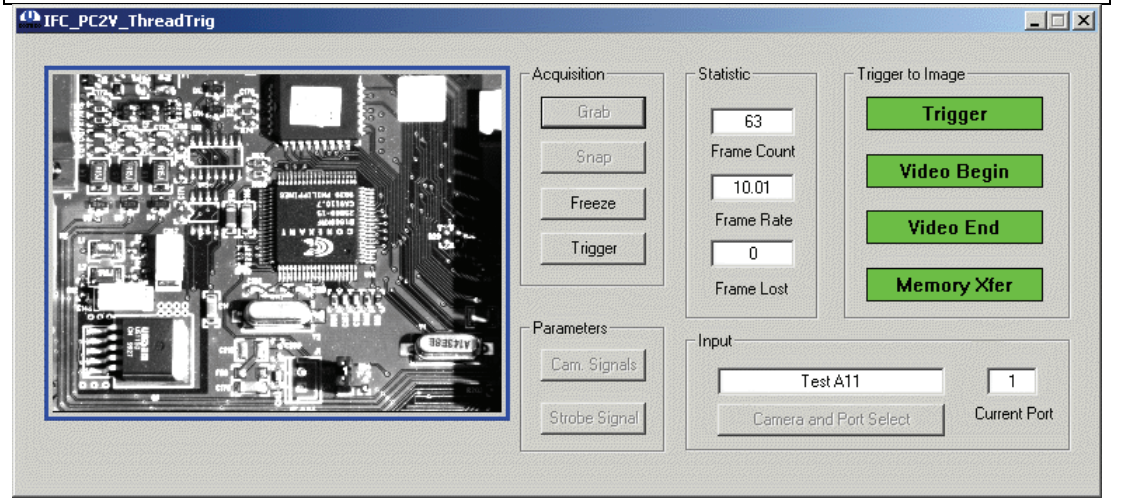
Title	Processing using a thread
Description	Shows how to do acquisition in the host buffer and the display as well as applying processing on every frame using a thread. The processing time is computed and shown. Processing function for this demo is simple thresholding.
Features	- Dialog-box based application - Camera and port selection - Grab or snap - SW trigger - Statistics indicators - Processing time indicator
Setup	- Any RS-170 or CCIR camera - Camera cable - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_ThreadProc**



IFC_PC2V_ThreadTrig

Title	Acquisition and display with external camera triggering
Description	The goal of this demo is to trigger the camera with an external trigger pulse instead of a free-running camera. This mode is useful to synchronize the images to an event and/or to capture fast moving objects. Using a progressive scan camera is recommended for fast moving objects. Study carefully the different trigger modes offered by your camera (edge pre-select,

	pulse width control, etc). Note that your config file must be in External Trigger mode. Demo uses visual indicators to represent the Trigger-To-Image reliability model. An indicator is available for each acquisition interrupt.
Features	- Dialog-box-based application - Camera and port selection - Grab or snap - SW trigger - Statistics indicators - Trigger To Image indicators - Camera signal timing (external trigger, frame reset, VSync, Strobe) edit box - Strobe edit box
Setup	- Progressive scan camera supporting asynchronous reset (camera must accept external VD and HD signals as well as camera trigger signals) - Camera cable - 1 PC2-Vision - Trigger source
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_ThreadTrig**



6Cam2Grab

Title	Fast camera switching from six synchronized cameras
Description	Synchronized acquisition from 2 groups of 3 cameras using fast camera switching
Features	MDI application with one window associated to each camera
Setup	- MDI-based application - 6 genlocked cameras - 2 camera cables - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ 6Cam2Grab**

IFC_PC2V_CamSwitch

Title	Fast camera switching one camera at a time
Description	Dynamic switching between (and up to) six synchronized cameras (XTAL).
Features	- Dialog-box-based application - Camera and port selection - Grab or snap - SW trigger - Statistics indicators - Trigger -to -image indicator
Setup	- From 1 to 6 genlocked cameras - 1 or 2 camera cables - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_CamSwitch**

IFC_PC2V_CamSwitchPlanarVertical

Title	Fast camera switching combined with vertical planar transfer
Description	Two blocks of three genlocked cameras acquiring in planar vertical mode using a single ring of buffers. Each buffer contains three images and is displayed in a single window where each camera image is on top of each other. The two blocks of three cameras are dynamically switched.
Features	- Dialog-box-based application - Frame rate indicator - Trigger presence indicator
Setup	- From 1 to 6 genlocked cameras

	- 1 or 2 camera cables
	- 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ IFC_PC2V_CamSwitchPlanarVertical**

IFC_PC2V_ManualCamSwitch

Title	**Manual camera switching**
Description	Up to 6 asynchronous cameras are acquired sequentially using SNAPs. This is typically used with PLL mode cameras (when cameras are not synchronized).
Features	- Dialog-box-based application
	- Independent config file selection for each of the 6 cameras
	- Frame rate indicator
	- Switching sequence selection
	- Trigger presence indicator
Setup	- From 1 to 6 cameras
	- 1 or 2 camera cables
	- 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ IFC_PC2V_ManualCamSwitch**

Switcher

Title	**Switcher using fast camera switching**
Description	Fast camera switching using up to 6 synchronized cameras
Features	- MDI-based application
	- Selection of switching sequence
	- Optional use of a single ring buffer
Setup	- From 1 to 6 genlocked cameras
	- 1 or 2 camera cables
	- 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ Switcher**

FrameDly

Title	**Frame Delay Readout (MDI)**
Description	Demonstrates how to acquire 6 cameras (maximum) simultaneously
Features	- SDI-based application
	- Camera presence selection

	- Save sequence to AVI format
Setup	- From 1 to 6 cameras supporting frame delay readout
	- 1 or 2 camera cables
	- 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ FrameDly**

IFC_PC2V_FrameDelay

Title	**Frame Delay Readout (Dialog-box-based)**
Description	Shows how to acquire from up to 6 cameras simultaneously in frame delay readout mode.
Features	- Dialog-box-based application
	- Grab or snap
	- SW trigger
	- Statistics indicators
	- Trigger-to-image indicator
Setup	- From 1 to 6 cameras supporting frame delay readout
	- 1 or 2 camera cables
	- 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_FrameDelay**

IFC_PC2V_FrameDelayPlanarVertical

Title	**Frame Delay Readout using Vertical Planar Transfer**
Description	Up to 6 cameras capture an image at the same moment and are subsequently acquired three at a time. They are stored in the host memory in a planar manner and displayed in a vertical planar manner.
Features	- Dialog-based application
	- 2 vertical planar displays
	- Selection of trigger source
	- Frame count and frame rate indicators
	- Trigger presence indicator
Setup	- From 1 to 6 cameras supporting frame delay readout
	- 1 or 2 camera cables
	- 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ IFC_PC2V_FrameDelayPlanarVertical**

IFC_PC2V_4Boards

Title	Acquisition with up to four PC2-Vision boards
Description	Shows how to acquire from up to 4 PC2-Vision boards within the same system. In this demo, each PC2-Vision requires one camera. Use serial numbers to identify which PC2-Vision board corresponds to which PCI slot.
Features	- Dialog-box-based application - Camera and port selection - Grab or snap - SW trigger - Statistics indicators - Serial number indicator for each card
Setup	- From 1 to 4 RS-170 or CCIR cameras - From 1 to 4 camera cables - From 1 to 4 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_4Boards**

Interrupt

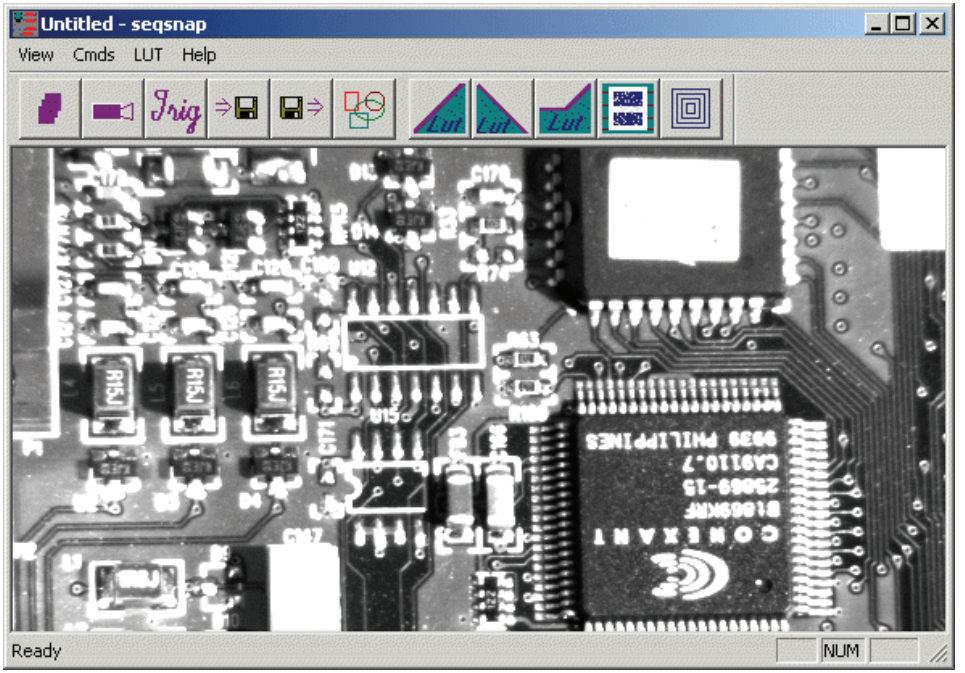
Title	Interrupt
Description	Shows how to register to the interrupts available on the PC2-Vision board. Camera trigger setup can be changed from within this application.
Features	- Uses **P2VTEST.TXT** for configuration - Support for all acquisition interrupts - External trigger configuration dialog - SW trigger generation
Setup	- Any RS-170 or CCIR camera on port 0 - Camera cable - 1 PC2-Vision - Source of external trigger
Project location	**Installation Directory\examples\PC2-Vision\IntrEx**

PulseGen

Title	Pulse Generator using Vixn
Description	Use the Vixn timer to generate high-precision pulses on the Parallel I/O output
Features	- Selection of pulse frequency - Selection of pulse width
Setup	- 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ PulseGen**

SeqSnap

Title	Sequential Snap
Description	Snaps a small number of images into host memory and replays them.
Features	- Uses **P2VTEST.TXT** for configuration - Snaps a short sequence of frames to host memory and replays this sequence. - Camera and port selection - Camera control for external trigger, frame reset, and strobe - Overlay demonstration - LUT demonstration - Window generator dialog - Saves AVI sequence
Setup	- Any camera - Camera cable - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\SeqSnap**

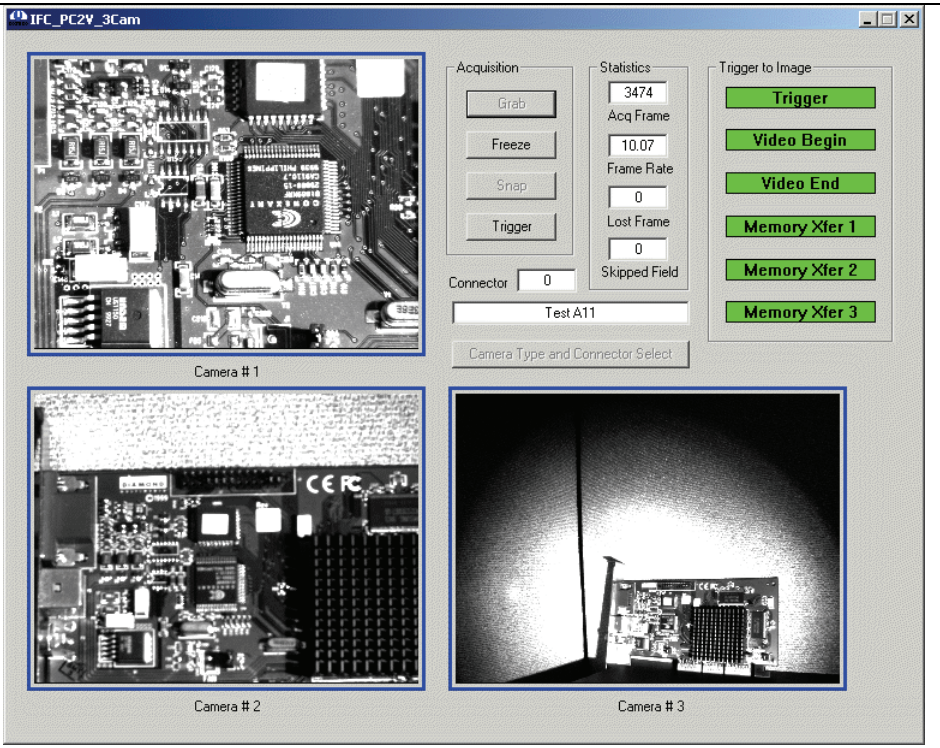


IFC_PC2V_Vixn

Title	Vixn versus regular callback latency and jitter comparison
Description	This demo shows how fast and constant a VIXN interrupt callback is achieved by comparing graphically the response time jitter of both a VIXN and a regular callback
Features	- Dialog-box-based application -Latency and jitter statistics for Vixn callbacks -Latency and jitter statistics for regular event callbacks -Frame rate indication
Setup	- Any camera - Camera cable - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ IFC_PC2V_Vixn**

IFC_PC2V_3Cam

Title	Acquisition from three genlocked cameras
Description	Simultaneous acquisition and display of three genlocked cameras in Planar transfer mode.
Features	- Camera and port selection - Grab or snap - SW trigger - Statistics indicators - Trigger To Image indicators
Setup	- 3 genlockable monochrome cameras (must accept external VD and HD signals) - Camera cable supporting three monochrome cameras - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\IFC_PC2V_3Cam**



IFC_PC2V_3CamPlanarVertical

Title	Three Cameras Acquisition with Planar Vertical Transfer
Description	Acquisition and display of 3 genlock monochrome cameras using a single ring and a single buffer for all 3 channels.
Features	-Dialog box-based application -Trigger-to-image reliability indicators -Statistics for frame count, frame rate, frame lost, frame not acquired, and frame not displayed. -Camera selection
Setup	- 3 genlockable monochrome cameras (must accept external VD and HD signals) - Camera cable supporting three monochrome cameras - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ IFC_PC2V_3CamPlanarVertical**

3Cam1Grab

Title	Three Cameras using a single Grab call
Description	Acquisition from 3 synchronized cameras
Features	- MDI-based application - Simultaneous display of 3 cameras outputs
Setup	- 3 genlockable monochrome cameras (must accept external VD and HD signals) - Camera cable supporting three monochrome cameras - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ 3Cam1Grab**

IFC_PC2V_3Cam1Ring

Title	Planar Acquisition from three cameras into a single ring buffer
Description	Simultaneous acquisition and display of three genlocked cameras in planar mode in a single ring of acquisition buffers. Planar mode means that the three images are at three different locations in memory. In this demo, IFC assumes that it is grabbing from a single RGB camera; but, the three colors signals could be, in fact, three monochrome signals coming from three cameras.
Features	-Dialog-box-based application -Grab statistics: frame count, frame rate, frame lost, frame not acquired, frame not displayed. -Trigger-to-image reliability indicators

	-Camera selection
Setup	- 3 genlockable monochrome cameras (must accept external VD and HD signals) - Camera cable supporting 3 monochrome cameras - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\ IFC_PC2V_3Cam1Ring**

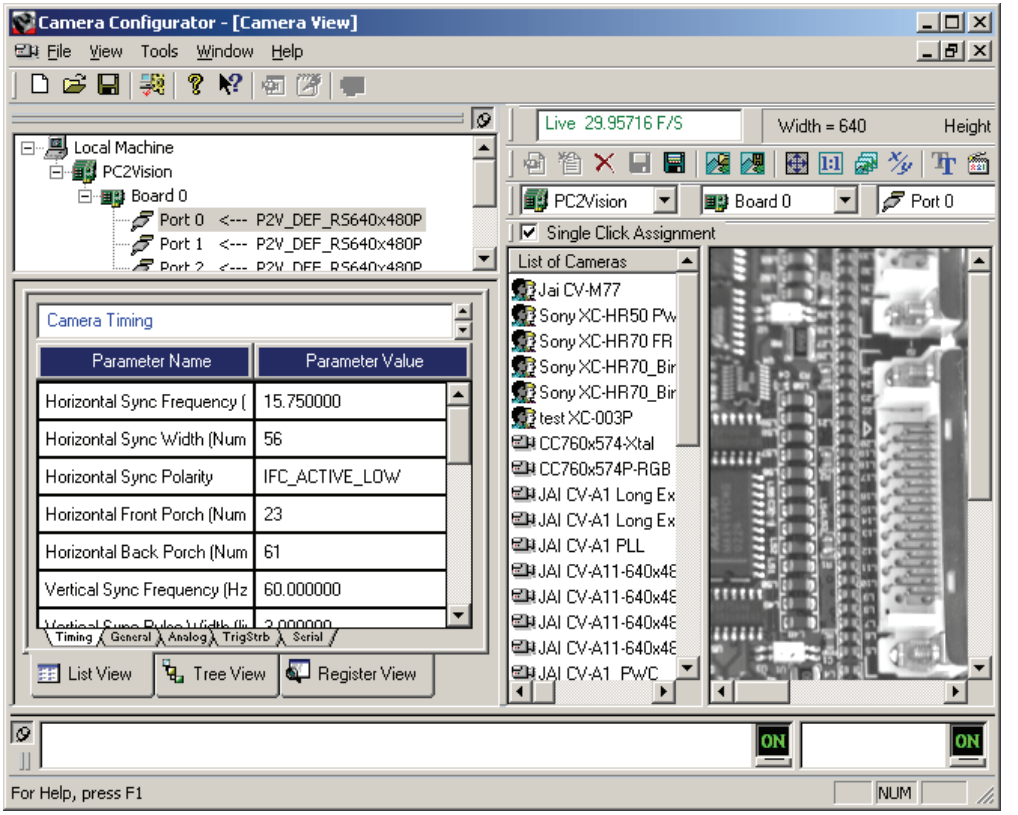
Grab3

Title	**Acquisition from three genlocked cameras**
Description	Simultaneous acquisition from three genlocked monochrome cameras with live display.
Features	Uses **P2VTEST.TXT** for configuration
Setup	- 3 genlockable monochrome cameras (must accept external VD and HD signals) - Camera cable supporting three monochrome cameras - 1 PC2-Vision
Project location	**Installation Directory\examples\PC2-Vision\Grab3**

Applying IFC Camera Configurator to PC2-Vision

Interfacing Cameras with IFC Camera Configurator

The IFC Camera Configurator® program is the camera interfacing tool for frame grabber boards supported by the IFC library, such as the PC2-Vision. Camera Configurator® generates the required camera configuration file (*yourconfig.txt*) based on the timing and control parameters entered.



The live acquisition window is an important tool within Camera Configurator®. It performs immediate verification on timing or control parameters without the need to run a separate acquisition program. An overview on how to use the Camera Configurator® is available via the IFC Configurator help file installed within the IFC folder accessed from the Start Menu.

This section provides information concerning interfacing between analog cameras and the PC2-Vision. Note that this applies to monochrome and RGB cameras.

Configuration Files Distributed with IFC

The IFC distribution CD-ROM includes a selection of supported camera configuration (.txt) files. Using the IFC Camera Configurator® program, your camera files can be reviewed or modified and corresponding .txt files quickly generated.

IFC Camera Application Library

TELEDYNE DALSA created and frequently updates a camera application library composed of application information and prepared camera configuration files. Refer to the “Camera Search” utility on the DALSA web site for application notes and camera configuration files that you can download.

A Note about Cameras

Many cameras have jumpers or a serial port to control their internal configuration. Make certain that they match your camera configuration file.

Interfacing Check List

Before undertaking the task of interfacing a camera from scratch using the Camera Configurator®:

- Confirm that DALSA has not already published an application note with camera configuration files (see "IFC Camera Application Library" on page 134).
- Check to see if the IFC installation has a similar type of camera file. A similar .txt file can be loaded into the Camera Configurator® where it would then be modified to match the timing and operating parameters for your camera and then saved as a new .txt camera configuration file.

Note: It is easier to find camera timing in free-running mode. Make certain that your camera operates correctly in free-running mode before attempting to use asynchronous reset mode.

Interfacing Free Running Cameras

Interfacing Camera to PC2-Vision with Camera Configurator®

To interface a new camera to your PC2-Vision, select a default camera (such as P2V_DEF_RS640x480P) and follow these steps.

General Acquisition Parameter Group

In Camera Configurator®, select the **General** tab in the "parameter view" on the left.

Since you are configuring a non-standard camera (standard cameras already have configuration files), set the following parameter:

```
Video Standard = IFC_VIDEO_STANDARD_NONE
```

Monochrome or RGB

Next, indicate if your camera is monochrome or RGB. In the "Parameter" section of the Camera Configurator®, select the **General** tab and go to *Color* parameter.

For monochrome:

```
Color = IFC_MONO    (8-bit monochrome)
```

For RGB:

```
Color = IFC_RGB     (32-bit zero-padded RGB)
```

Note: On PC2-Vision, the *Pixel Size* parameter is always 8-bits (read-only). For RGB video, each color plane has 8 bits.

Note: You can connect a maximum of two RGB cameras to one PC2-Vision. The first RGB camera uses ports 0, 1, and 2; the second camera uses ports 3, 4, and 5. The camera configuration file must be applied to port 0 or 3, respectively. Port 0 is blue, port 1 is green and port 2 is red for the first RGB camera. Port 3 is blue, port 4 is green and port 5 is red for the second RGB camera.

Interlaced or Non-interlaced

Select the scan method used by your camera: interlaced or non-interlaced scan.

For interlaced cameras:

```
Scan mode = IFC_ILACED
First Field in Frame = IFC_ODD_FIELD
```

For non-interlaced (progressive scan) cameras:

```
Scan mode = IFC_NILACED
First Field in Frame = IFC_NEXT_FIELD
```

Other parameters must be set to the default value:

```
Fields Processed = P2V_FIELD_PROCESS_ALL
Multi-tap mode = P2V_SINGLE_TAP
```

Cropper

The Cropper is used to define the region of interest (ROI) to capture within the active video region. This excludes the back and front porch. The ROI can be the whole frame size or a smaller area.

The Cropper applies to the horizontal and vertical active period. Therefore, the ROI refers to the image portion transferred to the host by the PC2-Vision. The cropped image area in the figure below illustrates this.

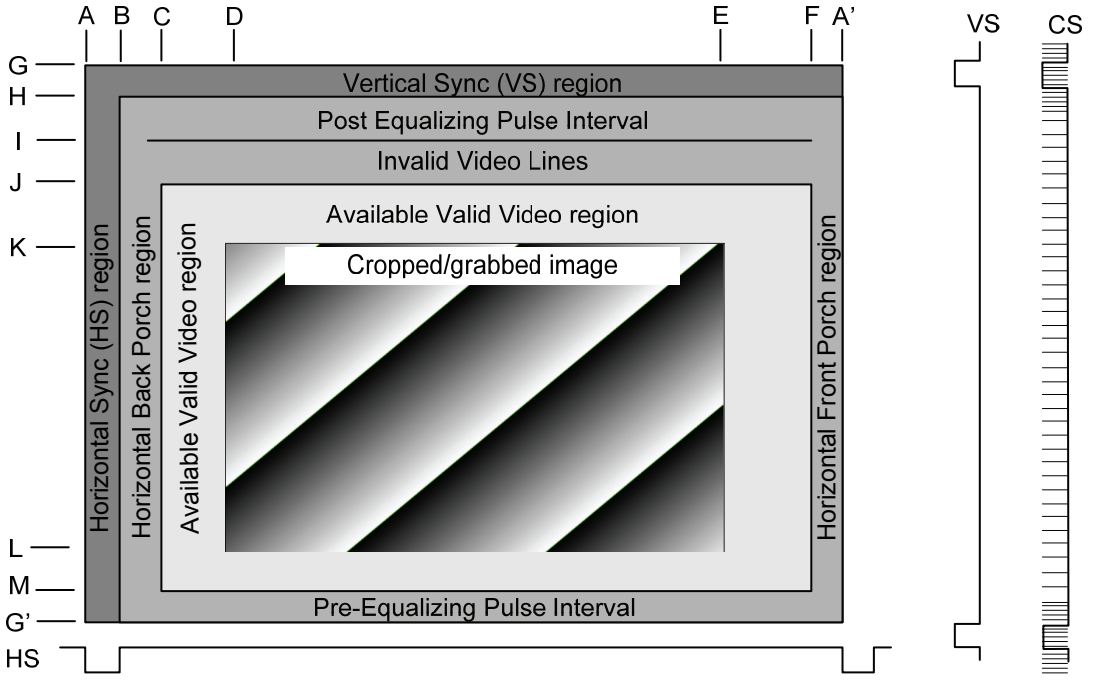


Figure 54: Cropper

Ref	Hardware signal	Description	Ref	Hardware signal	Description
A	sHLeadEdge_p	Horizontal Sync Leading Edge	M		First Line of Pre-Equalizing Pulse Interval
A'		Same as A + 1 line	(A,G)	sVLeadEdge_p	Vertical Sync Leading Edge (± ½ line)
B	sHTrailEdge_p	Horizontal Sync Trailing Edge aka Start of Horizontal Back Porch	(A, H)	sVTrailEdge	Vertical Sync Trailing Edge (± ½ line)
C		Horizontal Start of Valid Video	(D,K)	sSOFi_p	Start of Field (occur on first pixel of a grabbed field)
D	sSOL_p	First grabbed pixel of line (SOL: Start of Line) aka Horizontal Blank Stop	(D,K)	sSOF_p	Start of Frame (occur on first pixel of a grabbed frame)
E	sEOL_p	Last grabbed pixel of line (EOL: End of Line)	(D,K)	sSOF_p	Start of Transfer (only occur in first frame on first pixel of a grabbed stream)
E+1		Horizontal Blank Start	(E,L)	sEOFi_p	End Of Field (occur on last pixel of a grabbed field)
F		Start of Horizontal Front Porch	(E,L)	sEOF_p	End Of Frame (occur on last pixel of a grabbed frame)
G		First line of Vertical Sync	(E,L)	sEOF_p	End Of Transfer (only occur in last frame on last pixel of a grabbed stream)
G'		Same as G = 1 field/frame	A' – A		Line Width
H		First line of Post Equalizing Pulse Interval	B – A		HS Width
I		Last line of Post Equalizing Pulse Interval	A' – E + D		Horizontal Blank Width
J		First line of Valid Video provided by the camera	G' – G		Field/Frame Height/Width
K		First grabbed line of Field/Frame (usually K=J_	H – G		VS Height/Width
L		Last grabbed line of Field/Frame (usually L=M-1)	G' – L + K		Vertical Blank Height/Height/Width

Note: During camera configuration file development, it is better to use a window much smaller than the camera nominal size: the frame grabber needs to see at least the number of pixels defined by the window generator in order to correctly capture the image. By defining a smaller ROI, you ensure enough pixels are captured to fill the frame buffer.

Example1: Your camera has a nominal frame size of 1024 pixels by 768 lines and you want to capture the entire frame:

```
Horizontal Offset = 0
Width = 1024
Vertical Offset = 0
Height = 768
```

Example 2: You want to extract a ROI of 128 x 64 located 100 pixels to the right and 50 lines below the upper left corner of the image:

```
Horizontal Offset = 100
Width = 128
Vertical Offset = 50
Height = 64
```

Timing Parameter Group

Select the **Timing** tab in Camera Configurator®.

PLL, XTAL or VScan

In PLL (phase lock loop) mode, the frame grabber uses the timing information provided by the camera to digitize pixels. The HS (horizontal synchronization) and VS (vertical synchronization) information can be either:

- Embedded in the video signal (composite video).
  A single signal carries both sync and video.
- Provided on the same signal (composite sync).
  Two signals are required: csync and video.
- Provided on its own signal (separate sync).
  Three signals are required: hsync, vsync, and video.
- For a RGB camera, you can also define on which color channel the timing information is embedded (red, green, or blue).

In XTAL (crystal) mode, the frame grabber provides this timing to the camera. XTAL mode is also called Master Mode since the frame grabber is the timing master for the acquisition process.

In VScan (variable scan) mode, the camera provides the HS, VS, and pixel clock information to the frame grabber.

Note: It is possible with PC2-Vision to use a combination of Master Mode and External Sync. For example, the frame grabber can drive HD/VD to the camera but nonetheless use the composite video to extract the HS/VS used for digitization. DALSA recommends using synchronization from the composite video if the camera provides it.

For PLL mode:

```
Source of Input Sync. = P2V_SYNC_COMPOSITE_VIDEO  or P2V_SYNC_COMPOSITE_SYNC or
P2V_SYNC_SEPARATE_SYNC
Master HSync Enable = IFC_DISABLE
VSync Pulse Enable = P2V_VSYNC_DISABLE
Pixel Clock Source = P2V_PIXEL_CLOCK_INTERNAL
```

For XTAL mode:

```
Source of Input Sync. = P2V_SYNC_INTERNAL_SYNC
Master HSync Enable = IFC_ENABLE
VSync Pulse Enable = P2V_VSYNC_LINE_WIDTH
Pixel Clock Source = P2V_PIXEL_CLOCK_INTERNAL
```

Note: On the PC2-Vision, in XTAL mode with frame reset, the VD pulse is not automatically resynchronized to the frame reset pulse in contrast to the PC-Series, which does resynchronize to the frame reset pulse in XTAL mode with frame reset. To synchronize VD to frame reset, you must select *VSync Pulse Enable* = P2V_VSYNC_DISABLE.

For VScan Mode:

```
Source of Input Sync. = P2V_SYNC_SEPARATE_SYNC
Master HSync Enable = IFC_DISABLE
VSync Pulse Enable = P2V_VSYNC_DISABLE
Pixel Clock Source = P2V_PIXEL_CLOCK_EXTERNAL
```

Pixel Clock Timing

The Pixel Clock is used by the analog-to-digital converter (ADC) to digitize the video signal. The most important characteristic is the pixel clock frequency of your camera.

```
Pixel Clock Frequency = 'value from your camera datasheet (in MHz)'
Pixel Clock Polarity = IFC_RISING_EDGE
```

Horizontal Timing

The figure below reviews the basic horizontal timings of a typical analog camera. Note that the black level $\mathbf{V_P}$ is specific to the NTSC/RS-170/EIA video standard whereas other common video standards define black level as $\mathbf{V_T}$.

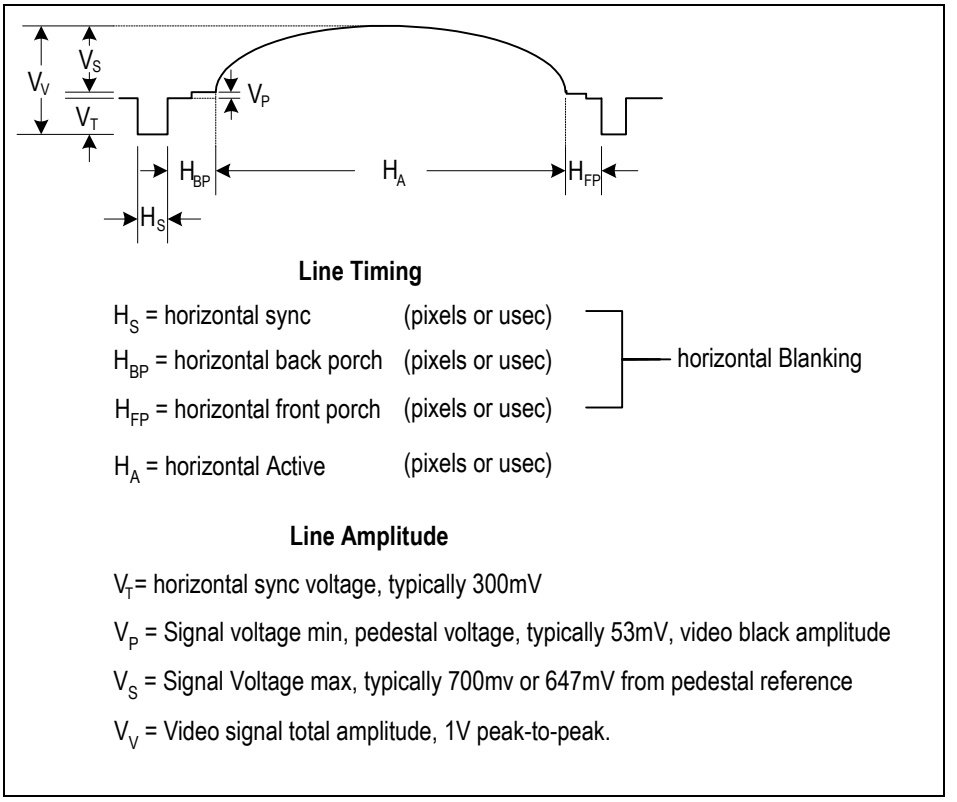


Figure 55: Horizontal Timing

PC2-Vision has the corresponding horizontal timing parameters:

Horizontal Sync Frequency: Line frequency of the camera. It is given by the following formula:

$$P\_HSYNC\_FREQ = \frac{1}{H_S + H_{BP} + H_A + H_{FP}}$$

Where H_S, H_{BP}, H_A and H_{FP} are expressed in seconds.

Horizontal Sync Width: horizontal sync pulse width in pixels. H_S in diagram above.

Horizontal Sync Polarity: Horizontal sync. pulse may be active high or active low. Active low is the most common.

Horizontal Front Porch: Horizontal front porch duration in pixels. H_{FP} in diagram above.

Horizontal Back Porch: Horizontal back porch duration in pixels. H_{BP} in diagram above. The horizontal back porch indicates the start of the frame to digitize. If its value is too low, a black bar appears on the left of the image. If the value is too high, you lose some of the first pixels in the image. If this information is not available from your camera datasheet, you may need to tweak a bit until you are right on the edge of the image.

Vertical Timing

The figure below reviews the basic vertical timings of a typical analog camera. The vertical synchronization shown in this example is called double-serration vertical sync, because the horizontal sync frequency is doubled during nine line periods. The double pulses are ignored by the frame grabber; therefore, the vertical sync parameter in the Camera Configurator® is always the number of true horizontal lines.

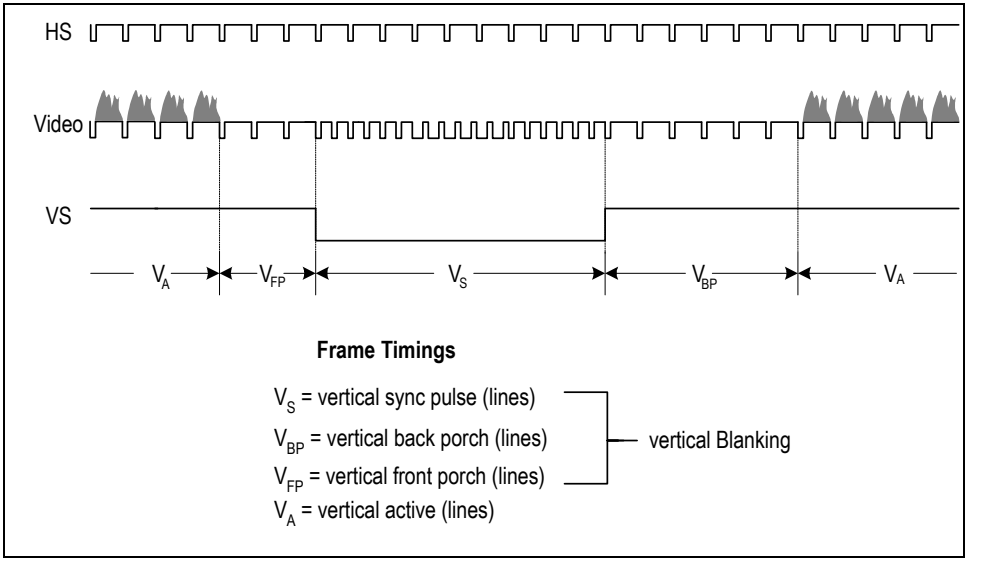


Figure 56: Vertical Timing

For interlaced video cameras, the HS to VS phase relationship changes from one field to the next (ODD/EVEN fields). This example represents the ODD field.

PC2-Vision has the corresponding vertical timing parameters:

Vertical Sync Frequency: Vertical sync. frequency. For interlaced scan cameras, this is the field rate (twice the frame rate). For progressive scan, this is the frame rate.
Vertical Sync Pulse Width: Vertical sync. pulse width in lines. V_S in diagram above.
Vertical Sync Polarity: Vertical sync. pulse may be active high or active low. Active low is the most common.
Vertical Front Porch: Vertical front porch duration in lines. V_{FP} in diagram above.
Vertical Back Porch: Vertical back porch duration in lines. V_{BP} in diagram above.

WEN Signal

Write Enable (WEN) is a signal available on some cameras to indicate the presence of valid data on the video signal. If it is available on your camera, WEN can be activated to replace the VS as the triggering condition to start digitizing a new frame.

```
WEN Input Enable = IFC_Enable
WEN Input Polarity = IFC_ACTIVE_HIGH or IFC_ACTIVE_LOW
WEN Vertical Offset = 'number of lines to skip after WEN'
```

Note: When WEN is activated, it is used internally by PC2-Vision to trigger the presence of a valid image. This is true for all sources of synchronization available (composite video, separate sync, and internal sync).

Analog Parameters Group

Select the **Analog** tab in Camera Configurator®.

Clamping

A programmable clamp pulse is used to establish the reference black video level. A region is defined on the horizontal back porch. This is required in order to assure proper image intensity.

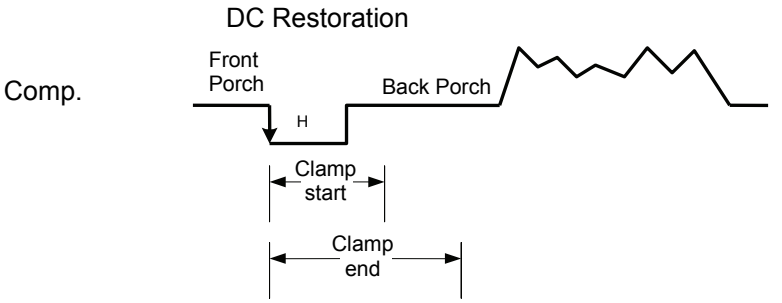


Figure 57: DC Restoration (Clamping)

```
Enable Clamping = IFC_ENABLE
Back Porch Clamp Start Delay = 'Clamp start' value on figure above
Back Porch Clamp End Delay = 'Clamp end' value on figure above
```

Note: If the clamp pulse region is defined in the HS sync pulse, the image will be too bright. If the clamp pulse region is defined in the active video, the image will generally be too dark. Clamp needs to be defined in the back porch to obtain the proper intensity.

Note: With Internal Sync mode, the horizontal reference is the edge of HD, as shown in "Figure 13: HD relation to HS" on page 33. With this synchronization scheme, clamp start and clamp end values refer to the first edge of HD, not to HS coming from composite video.

Anti-aliasing Filter

This low-pass filter is used to prevent aliasing during the digitization process. The Nyquist theorem states that to prevent aliasing, the maximal frequency of an analog signal must be less than twice the digitization rate. For example, if your pixel clock is 12MHz, you should enable a 6MHz filter to prevent aliasing.

PC2-Vision supports a 6MHz, 12MHz and a filter bypass option.

```
Low Pass Filter Control: Select appropriate filter for your Pixel Clock.
```

External Trigger and Strobe

PC2-Vision supports two external triggers and two strobe signals, one on each of the two MDR-36 camera connectors. In the Camera Configurator®, go to the **TrigStrb** tab.

Configuring the External Trigger

External Trigger Support

The external trigger is an input signal to the frame grabber indicating when to initiate an acquisition. PC2-Vision supports differential or TTL inputs.

Pinout:

MDR-36 pin 17: Ext_Trigger-
MDR-36 pin 18: Ext_Trigger+

Enabling Trigger

You first need to activate the external trigger:

```
Trigger Enable = IFC_ENABLE
```

Trigger Pulse

Next, define the physical attributes of the trigger.

Trigger Source: Source of the external trigger. Can be from first MDR-36 (IFC_EXT0_TRIG), second MDR-36 (IFC_EXT1_TRIG), connector holding the camera (IFC_EXT_AUTO_TRIG) or a software-generated trigger (IFC_SOFT_TRIG).

Trigger Polarity: Trigger can be detected on the rising edge (P2V_RISING_EDGE) or on the falling edge (P2V_FALLING_EDGE).

Trigger Debounce: This value indicates the minimal valid trigger pulse duration in µs. Any trigger pulse shorter than this value is rejected.

Frame Timing Related to Trigger

The remaining two trigger parameters are used to indicate trigger relation to the frames being acquired.

Frames per Trigger: Number of frames to capture when a valid external trigger is detected. This is normally set to 1 frame (each trigger fires the acquisition of one frame).

VSync to Wait before Grab: Indicates the number of VSync pulses to wait after a trigger before starting the acquisition. Normally set to 1 to start grabbing at the next VSync (grab the next valid frame).

Configuring the Strobe

Strobe Support

The strobe is an output signal from the frame grabber that is normally used to control a strobe light to illuminate the object while it is acquired.

Pinout:

MDR-36 pin 11: Strobe

The strobe is implemented using a timer. This timer can generate pulse duration up to 65 seconds.

Fast Strobe Mode

In Fast Strobe mode, the strobe pulse is sent immediately when the external trigger is detected. This is shown in following diagram. This mode is generally used for asynchronous reset cameras.

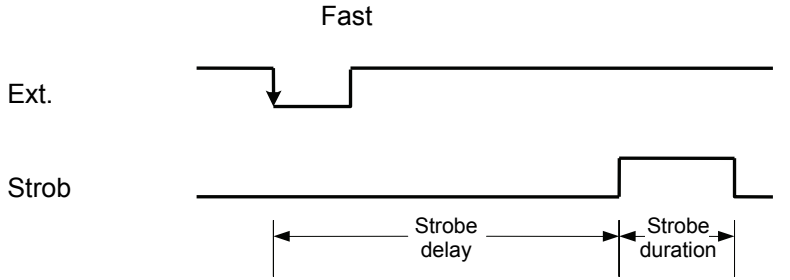


Figure 58: Fast Strobe

```
Strobe Output Enable = IFC_ENABLE
Strobe Mode = IFC_FAST_STROBE
Strobe Polarity: Active high (IFC_ACTIVE_HIGH) or active low (IFC_ACTIVE_LOW)
Strobe Duration: Duration of strobe pulse in µs
Strobe Delay = Defines the delay from Ext. Trigger before firing the strobe pulse.
Strobe Aligned on Horz Sync: Enable if you want strobe pulse to be aligned on HS
```

Note: PC2-Vision Fast Strobe mode does not support an exclusion region.

Slow Strobe Mode

In Slow Strobe mode, the strobe pulse is sent after the first VS following the external trigger. In this case, the strobe delay represents the amount of time after VS before the strobe is fired, as shown in diagram below. This mode is generally used for free-running cameras.

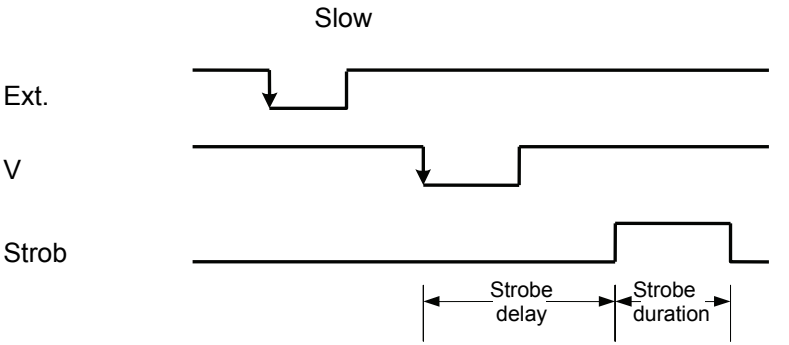


Figure 59: Slow Strobe

```
Strobe Output Enable = IFC_ENABLE
Strobe Mode = IFC_SLOW_STROBE
Strobe Polarity: Active high (IFC_ACTIVE_HIGH) or active low (IFC_ACTIVE_LOW)
Strobe Duration: Duration of strobe pulse in µs.
Strobe Delay: Define the delay from VS before firing the strobe pulse.
Strobe Aligned on Horz Sync: Enable if you want strobe pulse to be aligned on HS
```

Caution: the strobe pulse is aligned to the VS used by the PC2-Vision board. 'Source of Sync' of P2V_SYNC_COMPOSITE_VIDEO means that the VS is coming from the camera. 'Source of Sync' of P2V_SYNC_INTERNAL_SYNC means that the VS is generated by PC2-Vision. When 'VSync Pulse Enable' is set to P2V_VSYNC_LINE_WIDTH, the master mode engine generating VS is asynchronous to the external trigger. Your strobe pulse might therefore shift in time.

Asynchronous Reset Mode

Theory of Operation for PC2-Vision

Asynchronous Reset mode uses one (or more) pulse sent to the camera to control the exposure and acquisition.

Note: In Asynchronous Reset mode with synchronization on Internal Sync activated, use P2V_VS_PULSE_ENABLE = IFC_VSYNC_DISABLE in order for the frame reset and internal VS pulse to be synchronized together. Otherwise, your image will shift vertically while grabbing since the Master Mode VS is not synchronized to frame reset.

Pulse Width Control Mode

In Pulse Width Control, the integration time of the CCD is controlled by the duration of the frame reset pulse sent to the camera. This pulse can be optionally aligned to HS.

The frame reset is implemented using a timer. This timer can generate pulse duration up to 65 seconds.

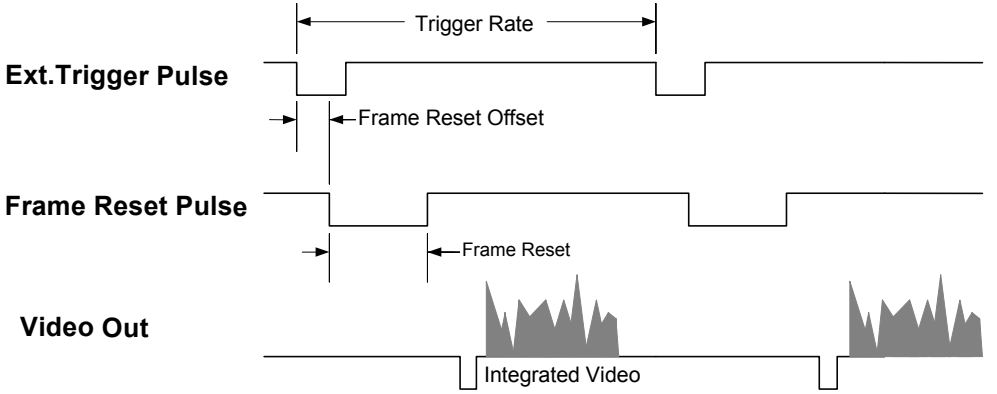


Figure 60: Pulse Width Control

The following parameters are located under the **TrigStrb** tab:

```
Frame Reset Mode = IFC_ENABLE
Frame Reset Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH
Frame Reset Offset: Offset in µs after external trigger pulse before asserting frame
reset.
Frame Reset Size: Duration in µs of frame reset pulse.
Add Frame Reset to VSync = IFC_DISABLE
Frame Reset Aligned on Horz Sync = IFC_ENABLE
```

Refer to "Configuring the External Trigger" on page 144 section to set external trigger parameters.

Edge Pre-Select Mode

Edge Pre-Select is equivalent to "pulse width control" except for one characteristic: the exposure period is governed by a camera setting (and not by the duration of the frame reset pulse). The first edge of the frame reset pulse triggers the camera.

Restart-Reset/Long Time Exposure Mode in Free Running

The integration time is controlled by the interval between two VD pulses. Vertical sync and horizontal sync are input to the camera.

The VSync is implemented using a timer. This timer can generate pulse duration up to 65 seconds.

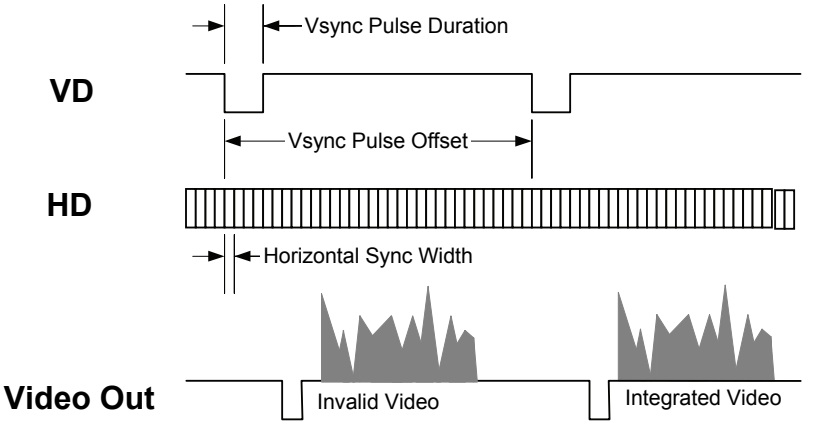


Figure 61: Restart-Reset/Long Time Exposure (Free Running)

The VSync pulse parameters are located under the **Timing** tab. They control the VD pulse.

VSync Pulse Enable = P2V_VSYNC_TIME_WIDTH
VSync Pulse Offset: Delay between VD pulses sent to camera. This corresponds to the frame rate for non-interlaced cameras.
VSync Pulse Duration: Size of the VD pulse in µs.
Add VSync to Frame Reset = IFC_DISABLE
Vertical Sync Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH
VSync Aligned on Horz Sync = IFC_ENABLE

The horizontal timing parameters are located under the **Timing** tab. They control HD pulses.

Master HSync Enable = IFC_ENABLE
Horizontal Sync Frequency: Line frequency of the camera in kHz.
Horizontal Sync Width: Size of the HD pulse in number of pixels.
Horizontal Sync Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH

Restart-Reset/Long Time Exposure Mode with External Trigger

An external trigger fires the acquisition process. Two timers (VS and Frame Reset) must be combined onto the VS signal to define the exposure. Each timer is independent and is fired by the external trigger.

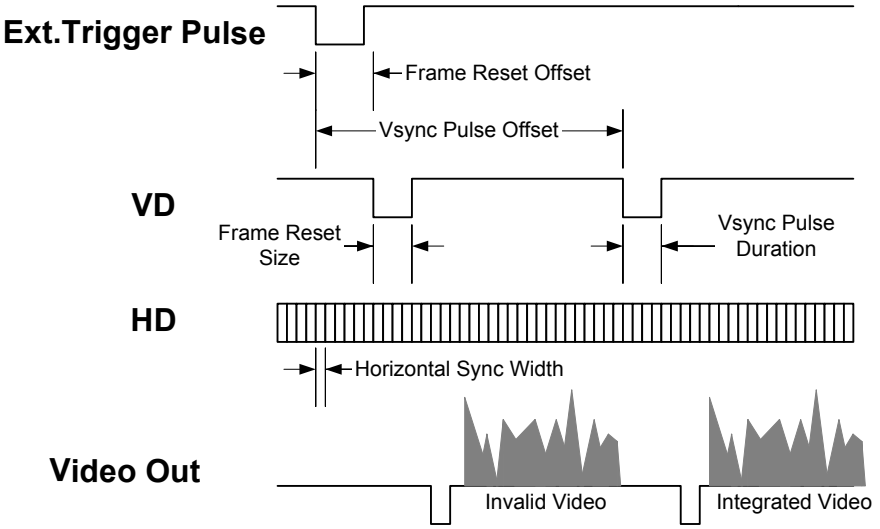


Figure 62: Restart-Reset/Long Time Exposure Mode (External Trigger)

Frame reset parameters are located under the **TrigStrb** tab. They control the first VD pulse.

```
Frame Reset Mode = IFC_ENABLE
Frame Reset Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH (same as VS polarity)
Frame Reset Offset: Offset in µs after external trigger before asserting first VD
pulse.
Frame Reset Size: Size of the first VD pulse in µs.
Add Frame Reset to VSync = IFC_ENABLE
Frame Reset Aligned on Horz Sync = IFC_ENABLE
```

VSync pulse parameters are located under the **Timing** tab. They control the second VD pulse.

```
VSync Pulse Enable = P2V_VSYNC_TIME_WIDTH
VSync Pulse Offset: Offset in µs after external trigger before asserting second VD
pulse.
VSync Pulse Duration: Size of the second VD pulse in µs.
Add VSync to Frame Reset = IFC_DISABLE
Vertical Sync Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH (same as frame reset
polarity)
VSync Aligned on Horz Sync = IFC_ENABLE
```

Horizontal timing parameters are located under the **Timing** tab. They control HD pulses.

```
Master HSync Enable = IFC_ENABLE
Horizontal Sync Frequency: Line frequency of the camera in kHz.
Horizontal Sync Width: Size of the HD pulse in number of pixels.
Horizontal Sync Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH
```

Refer to "Configuring the External Trigger" on page 144 to set external trigger parameters.

E-Donpisha/Start-Stop Trigger Mode

Exposure time starts on the frame reset signal and ends on VD. The frame grabber drives both of these signals.

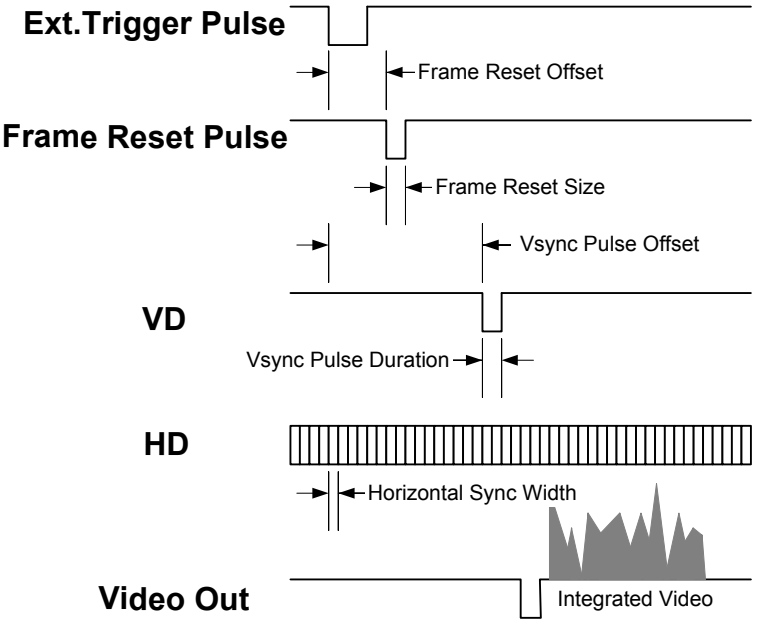


Figure 63: E-Donpisha/Start-Stop Trigger

Frame reset parameters are located under the **TrigStrb** tab. They control the frame reset pulse.

```
Frame Reset Mode = IFC_ENABLE
Frame Reset Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH
Frame Reset Offset: Offset in µs after external trigger before asserting frame reset.
Frame Reset Size: Size of the frame reset pulse in µs.
Add Frame Reset to VSync = IFC_DISABLE
Frame Reset Aligned on Horz Sync = IFC_ENABLE
```

VSync pulse parameters are located under the **Timing** tab. They control the VD pulse.

```
VSync Pulse Enable = P2V_VSYNC_TIME_WIDTH
VSync Pulse Offset: Offset in µs after external trigger before asserting VD pulse.
VSync Pulse Duration: Size of the VD pulse in µs.
Add VSync to Frame Reset = IFC_DISABLE
Vertical Sync Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH
VSync Aligned on Horz Sync = IFC_ENABLE
```

Horizontal timing parameters are located under the **Timing** tab. They control HD pulses.

```
Master HSync Enable = IFC_ENABLE
Horizontal Sync Frequency: Line frequency of the camera in kHz.
Horizontal Sync Width: Size of the HD pulse in number of pixels.
Horizontal Sync Polarity = IFC_ACTIVE_LOW or IFC_ACTIVE_HIGH
```

Refer to "Configuring the External Trigger" (on page 144) section to set external trigger parameters.

Serial Port

Serial Port Selection

The serial port must be mapped to the appropriate MDR-36 connector in order to control the camera. Under the **General** tab:

```
Select Active Uart Port = P2V_UART_PORT_AUTO to use same connector as the active
camera (first MDR-36 for camera 1, 2, and 3; second MDR-36 for port 4, 5, and 6)
P2V_UART_PORT_CON1  for first MDR-36 (J1); P2V_UART_PORT_CON2 for second MDR-36 (J2).
```

Additional Information

Note on Analog Camera Timing Relationships

For analog cameras, the following formulas show the relationship between the PCLK parameter and the Horizontal and Vertical total. These values must be accurate if the acquisition board drives the synchronization signals to the camera (board is in XTAL/Master Mode).

- The HS and VS signal frequencies are:

$$\frac{1}{HS_{freq}} = \frac{1}{PCLK_{freq}} * H_{total} \qquad \frac{1}{VS_{freq}} = \frac{1}{HS_{freq}} * V_{total}$$

To interface a video camera, the video timing concepts presented are now matched to the camera specifications and that data is entered into Camera Configurator®.

- The pixel clock frequency is critical for a 1:1 aspect ratio capture from analog cameras. But sub-sampling and over-sampling is easily achieved by changing the pixel clock frequency.

Overview of Video Bandwidth and System Limitations

Some high resolution/high frame rate cameras can output more data than can be transferred through the host computer's PCI bus. A successful imaging application must account for the camera data bandwidth and possibly control frame rate or image resolution to bring the bandwidth requirements to within the system's limitations.

Bandwidth is defined in two different ways. Peak bandwidth is the highest data rate occurring at any time during the data transfer. The average bandwidth is the amount of data per unit of time being transferred.

Each is calculated as follows:

- Peak Bandwidth (MBps) = Pixel Clock Frequency *Bpp *nb channels
- Average Bandwidth (MBps) = Frame Width *Frame Height *Frame Rate *Bpp
- where:
- MBps = MegaBytes per second

- Bpp = Bytes per pixel
- nb = number of …

When the bandwidth required by the frame grabber exceeds the capacity of the PCI 32-bit bus, the following techniques can reduce and optimize the average bandwidth.

Bandwidth Reduction Techniques

- A linear relationship exists between the average bandwidth required and the acquisition image height. For example, if four cameras of 1K x 1K, at some frame rate, need to transfer 160MB per/second of data, those four cameras at a 512 x 1K resolution will only need a bandwidth of 80MB per/second, which is now within the capability of the PCI-32 bus.
- For RGB cameras, pixel information is normally padded to 32-bits for the PC2-Vision. Using the Planar Transfer mode, where each color plane is sent to its own host buffer, can reduce PCI traffic by 25%□3-bytes to transfer (RGB) instead of 4 (0RGB).

Bandwidth Optimization Techniques

The following techniques are suggestions for applications that require all possible optimizations from the host system. Implementing these suggestions require a thorough understanding of your computer system setup and its BIOS controls.

- Allocate a separate IRQ for the frame grabber. BIOS settings can be used to manually assign the IRQ number to a particular PCI slot. As an alternative, the Window Device Manager can be used to force a specific IRQ to a specific PCI slot.
- Minimize the PCI latency timer in the BIOS setting; the value is given in CLK cycles.
- Use a high-performance AGP VGA board to decrease the image display system overhead when live acquisition is required.
- Avoid any hard drive write/read operations and network access through PCI LAN interfaces during intensive image transfers by the frame grabber.

Important: Some computer systems do not provide the BIOS controls described. Review your system manual.

PCVision IFC Parameter Comparison

Overview

The following tables compare IFC parameters between PCVision and PC2-Vision. They are intended to help someone familiar with PCVision to create config files for PC2-Vision. Parameters on the same line control equivalent functionality on their respective board. For a complete description of each parameter, please refer to the IFC-SDK™ Software manual.

Timing Parameters

PCVision Param	Values	PC2-Vision Param	Values
P_TIMING_SRC	IFC_PLL_STRIPPED_SYNC IFC_XTAL_SEPARATE_SYNC_OUT IFC_XTAL_COMPOSITE_SYNC_OUT IFC_VARIABLE_SCAN	P2V_SYNC_SOURCE	P2V_SYNC_COMPOSITE_VIDEO P2V_SYNC_COMPOSITE_SYNC P2V_SYNC_SEPARATE_SYNC P2V_SYNC_INTERNAL_SYNC P2V_SYNC_RED P2V_SYNC_GREEN P2V_SYNC_BLUE
Use XTAL mode on PCVision		P2V_MASTER_HSYNC	IFC_DISABLE IFC_ENABLE
Use XTAL mode on PCVision		P2V_VS_PULSE_ENABLE	P2V_VSYNC_DISABLE P2V_VSYNC_LINE_WIDTH P2V_VSYNC_TIME_WIDTH
P_PIXEL_CLK_FREQ	Range: 1.0 to 20.0MHz step size of 0.00001MHz	P_PIXEL_CLK_FREQ	Range: 1 to 40MHz steps size 0.00001MHz (10Hz)
P_PIXEL_CLK_POLARITY	IFC_FALLING_EDGE IFC_RISING_EDGE	P_PIXEL_CLK_POLARITY	IFC_RISING_EDGE
Use IFC_VARIABLE_SCAN		P_PIXEL_CLK_SIGNAL_TYPE	P2V_PIXEL_CLOCK_INTERNAL P2V_PIXEL_CLOCK_EXTERNAL
P_LEN_POLARITY	IFC_FALLING_EDGE IFC_RISING_EDGE	Use P_HSYNC_POLARITY	
P_FEN_POLARITY	IFC_FALLING_EDGE IFC_RISING_EDGE	Use P_VSYNC_POLARITY	
AMV_FIELD_SRC	AMV_VIDEO_STRIPPED_FLD AMV_LEN_AND_FEN_DETECTED_FLD	Use P2V_SYNC_SOURCE	
AMV_FIELD_SHIFT	AMV_CROP_HALFLINE AMV_FLDSHFT_NORM	*Use Cropper to remove halfline*	
P_HSYNC_FREQ	Range: 10.0 to 50.0KHz step size of 0.00001KHz.	P_HSYNC_FREQ	Range 7.0 to 50.0KHz in steps of 0.00001KHz (0.01Hz)
P_HSYNC_WIDTH	Range: 0.1 to 100.0 µs step size of 0.00001 µs	P_HSYNC_WIDTH	Range 1 to 400 pixels in steps of 1 pixel
P_HSYNC_POLARITY	IFC_ACTIVE_HIGH IFC_ACTIVE_LOW	P_HSYNC_POLARITY	IFC_ACTIVE_LOW IFC_ACTIVE_HIGH

P_VSYNC_FREQ	Range: 10.0 to 100.0Hz step size of 0.00001Hz	P_VSYNC_FREQ	Range: 2.0 to 1,000.0Hz in steps of 0.00001Hz
P_VSYNC_WIDTH	Range 1.0 to 20.0ms step size of 0.5ms	P_VSYNC_WIDTH	Range 1 to 20 lines in steps of 1 line
P_VSYNC_POLARITY	IFC_ACTIVE_HIGH IFC_ACTIVE_LOW	P_VSYNC_POLARITY	IFC_ACTIVE_LOW IFC_ACTIVE_HIGH
P_NUM_EQ_PULSES_FPORCH	Range: 0 to 10 step size of 1	P_NUM_EQ_PULSES_FPORCH	Range 0 to 100 lines in steps of 1 line
P_NUM_EQ_PULSES_BPORCH	Range: 0 to 10 step size of 1	P_NUM_EQ_PULSES_BPORCH	Range 0 to 100 lines in steps of 1 line
P_EQ_PULSE_WIDTH	Range: 0.1 to 50.0 us in 0.00001 µs steps	*No equivalent on PC2-Vision*	
P_SERR_PULSE_WIDTH	Range: 0.1 to 50.0 us in 0.00001 µs steps	*No equivalent on PC2-Vision*	
No equivalent on PCVision		P2V_VS_PULSE_OFFSET	Range: 0 to 65535000 µs step size of 1 µs
No equivalent on PCVision		P2V_VS_PULSE_DURATION	Range: 1 to 65535000 µs step size of 1 µs
Always enabled on PCVision		P2V_VSYNC_ALIGN_ON_HS	IFC_DISABLE IFC_ENABLE
No equivalent on PCVision		P2V_ADD_VSYNC_TO_FRAME_RESET	IFC_DISABLE IFC_ENABLE
AMV_PTG_VSYNC_OUT_EN	IFC_DISABLE IFC_ENABLE	P2V_VSYNC_OUT_ENABLE	IFC_DISABLE IFC_ENABLE
Always enabled on PCVision		P2V_VSYNC_OUT_ALL_CONN	IFC_DISABLE IFC_ENABLE
No equivalent on PCVision		P_WEN_ENABLE	IFC_DISABLE IFC_ENABLE
No equivalent on PCVision		P_WEN_POLARITY	IFC_ACTIVE_LOW IFC_ACTIVE_HIGH
No equivalent on PCVision		P_WEN_VERTICAL_OFFSET	Range: 0 to 256 lines step size 1 line

General Parameters

PCVision Param	Values	PC2-Vision Param	Values
P_PIXEL_SIZE	8-bits per pixel	P_PIXEL_SIZE	Range: 1 to 32-bits
P_FIRST_FIELD_STAT	IFC_EVEN_FIELD IFC_ODD_FIELD	*No equivalent on PC2-Vision*	
P_FIRST_FIELD_CMD	IFC_NEXT_FIELD IFC_EVEN_FIELD IFC_ODD_FIELD	P_FIRST_FIELD_CMD	IFC_NEXT_FIELD IFC_EVEN_FIELD IFC_ODD_FIELD
P_SCAN_MODE_STAT	IFC_NILACED IFC_ILACED	P_SCAN_MODE_STAT	IFC_NILACED IFC_ILACED
P_PIXEL_COLOR	IFC_MONO	P_PIXEL_COLOR	IFC_MONO IFC_RGB IFC_RGB_PLANAR

No equivalent on PCVision		P2V_MULTITAP_MODE	P2V_SINGLE_TAP P2V_2TAP_ILACE_FIXED
No equivalent on PCVision		P2V_PLANAR_MODE	P2V_PLANAR_DISABLED P2V_PLANAR_HORZ P2V_PLANAR_VERT
P_INPUT_LUT1_FILE	filename	P_INPUT_LUT1_FILE	filename
AMV_INPORT_POLARITY	IFC_FALLING_EDGE IFC_RISING_EDGE	Use CICapMod ::InportInterruptPolarity	
AMV_INPORT	IFC_LEVEL_HIGH IFC_LEVEL_LOW	Use CICapMod::InportVal	
AMV_OUTPORT	IFC_LEVEL_HIGH IFC_LEVEL_LOW	Use CICapMod::OutportVal	
AMV_YCRCB_MONO_ACQ	IFC_DISABLE IFC_ENABLE	Use IfxCreateImgConn with IFC_YCRCB_SINK	
P_HORZ_OFF	Range: 1 to 1024 pixels step size of 1	P2V_HORZ_BACK_PORCH + P_HORZ_OFF	Range 0 to 400 pixels in steps of 1 pixel Range: 0 to 2044 pixels step size 1 pixel
No equivalent on PCVision		P2V_HORZ_FRONT_PORCH	Range 0 to 400 pixels in steps of 1 pixel
P_WIDTH_PIXELS	Range: 8 to 16384 pixels step size of 8 pixels	P_WIDTH_PIXELS	Range: 4 to 2048 pixels step size 4 pixels
P_VERT_OFF	Range: 1 to 1024 lines step size of 1 line	P_VERT_OFF	Range: 0 to 2047 lines step size 1 line
P_HEIGHT_PIXELS	Range: 1 to 4096 lines step size of 1 line	P_HEIGHT_PIXELS	Range: 1 to 2048 lines step size 1 line
No equivalent on PCVision		P_VIDEO_STANDARD	IFC_VIDEO_STD_NTSC IFC_VIDEO_STD_PAL IFC_VIDEO_STD_NONE
No equivalent on PCVision		P2V_FIELD_PROCESS	P2V_FIELD_PROCESS_ALL P2V_FIELD_PROCESS_ODD_ONLY P2V_FIELD_PROCESS_EVEN_ONLY
No equivalent on PCVision		P2V_SELECT_UART_PORT	P2V_UART_PORT_AUTO P2V_UART_PORT_CON1 P2V_UART_PORT_CON2

Analog Parameters

PCVision Param	Values	PC2-Vision Param	Values
P_ANALOG_GAIN	Valid gain settings are: 1.0 and 1.5	*No analog gain on PC2-Vision, use brightness/contrast*	
AMV_LOW_PASS_FILTER_EN	IFC_DISABLE IFC_ENABLE	P2V_LOW_PASS_FILTER	P2V_LPF_6_5_MHZ P2V_LPF_12_MHZ P2V_LPF_BYPASS
AMV_NREF_CONTROL + AMV_PREF_CONTROL	Range: 0 to 1.2 volts step size of 0.01875 Range: 0 to 2 volts step size of 0.03125	P_BRIGHTNESS + P_CONTRAST	Range: 0 to 100 in steps of 0.1 Range: 0 to 100 in steps of 0.1
AMV_EDONPISHA_MODE	IFC_DISABLE IFC_ENABLE	*Use frame reset and VSync pulse*	
P_CLAMP_HSYNC_EDGE	IFC_FALLING_EDGE IFC_RISING_EDGE	*Clamping always defined on the active edge of HSync for PC2-Vision*	
P_CLAMP_OFFSET_TIME	Range: 0 to 50 µs step size of 0.00001 µs	P2V_CLAMP_START + P2V_CLAMP_END	Range: 0.1 µs to 51.1 µs step size of 0.025 µs (25ns) Range: 0.1 µs to 51.1 us step size of 0.025 µs (25ns)
AMV_CLAMP_SOURCE	AMV_AUTOCLAMP AMV_PROGCLAMP	P_CLAMP_MODE	IFC_ENABLE

Trigger and Strobe Parameters

PCVision Param	Values	PC2-Vision Param	Values
P_TRIGGER_ENABLE	IFC_DISABLE IFC_ENABLE	P_TRIGGER_ENABLE	IFC_DISABLE IFC_ENABLE
P_TRIGGER_SRC	IFC_EXT0_TRIG IFC_SOFT_TRIG	P_TRIGGER_SRC	IFC_SOFT_TRIG IFC_EXT0_TRIG IFC_EXT1_TRIG IFC_EXT_AUTO_TRIG
P_TRIGGER_POLARITY	IFC_ACTIVE_HIGH IFC_ACTIVE_LOW	P_TRIGGER_POLARITY	IFC_FALLING_EDGE IFC_RISING_EDGE
P_TRIGGER_STATE	AMV_TRGCYC_IDLE AMV_TRGCYC_ACTIVE	*No equivalent on PC2-Vision*	
P_GEN_SW_TRIGGER	Range: 0 to 1 step size of 1	P_GEN_SW_TRIGGER	range 0 to 1 step size 1
No equivalent on PCVision		P_FRAMES_PER_TRIGGER	Range: 1 to 1000 frames step size of 1 frame
No equivalent on PCVision		P_TRIGGER_DEBOUNCE	Range: 1 to 255 µs step size 0.1 µs
No equivalent on PCVision		P2V_VSYNC_WAIT_COUNT	Range: 0 to 255 step size 1
AMV_SKIP_FIELD_MODE	IFC_DISABLE IFC_ENABLE	*No equivalent on PC2-Vision*	
P_FRAME_RESET_MODE	IFC_DISABLE IFC_ENABLE	P_FRAME_RESET_MODE	IFC_DISABLE IFC_ENABLE

P_FRAME_RESET_POLARITY	IFC_ACTIVE_HIGH IFC_ACTIVE_LOW	P_FRAME_RESET_POLARITY	IFC_ACTIVE_LOW IFC_ACTIVE_HIGH
P_FRAME_RESET_OFFSET	Range: 1 to 256 lines step size of 1 line	P_FRAME_RESET_OFFSET	Range: 0 to 65535000 µs step size of 1 µs
P_FRAME_RESET_SIZE	IFC_FRAME_RESET_OFFSET_PERIOD IFC_FRAME_RESET_ONE_LINE	P_FRAME_RESET_SIZE	Range: 1 µs to 65535000 µs step size of 1 µs
Always enabled on PCVision		P2V_FRAME_RESET_ALIGN_ON_HS	IFC_DISABLE IFC_ENABLE
AMV_FRAME_RESET_ON_VSYNC_OUTPUT	IFC_DISABLE IFC_ENABLE	P2V_ADD_FRAME_RESET_TO_VSYNC	IFC_DISABLE IFC_ENABLE
P_STROBE_MODE	IFC_FAST_STROBE IFC_SLOW_STROBE	P_STROBE_MODE	IFC_FAST_STROBE IFC_SLOW_STROBE
P_STROBE_POLARITY	IFC_ACTIVE_HIGH IFC_ACTIVE_LOW	P_STROBE_POLARITY	IFC_ACTIVE_HIGH IFC_ACTIVE_LOW
P_STROBE_DELAY	Range: 1 to 64 lines step size of 1 line	P_STROBE_DELAY	Range: 0 µs to 65535000 µs step size of 1 µs
P_STROBE_ENABLE	IFC_DISABLE IFC_ENABLE	P_STROBE_ENABLE	IFC_DISABLE IFC_ENABLE
No equivalent on PCVision		P_STROBE_DURATION	Range 10 µs to 65535000 µs step size 1 µs
Always enabled on PCVision		P2V_STROBE_ALIGN_ON_HS	IFC_DISABLE IFC_ENABLE

Troubleshooting

Overview

This section provides suggestions for resolving installation or usage problems that may be encountered with the PC2-Vision due to the constant changing nature of computer equipment and operating systems. Note that information provided within this section will be updated with the latest information TELEDYNE DALSA can provide for each manual version released.

If you require help and need to contact TELEDYNE DALSA Technical Support, make detailed notes on your installation and/or test results for our technical support to review.

Tools

Windows Event Viewer

Windows Event Viewer (**Computer Management • System Tools • Event Viewer**) lists various events that have taken place during the OS boot sequence. If a driver generates an error it will normally log an entry in the event list. The Computer Management utility is available by right-clicking **My Computer** in the Explorer window (or desktop icon) and selecting **Manage** in the pop-up menu.

Device Manager Program

The Device Manager program provides a convenient method of collecting information about the installed PC2-Vision. System information, such as operating system, computer CPU, system memory, PCI configuration space, as well as PC2-Vision firmware information can be written to a text file (default file name: **BoardInfo.txt**).

Execute the program using the Windows Start Menu shortcut **Start • All Programs • DALSA • PC2-Vision Device Driver • Device Manager**. If the Device Manager program does not run, it will exit with a message that the board was not found. Since the PC2-Vision board must have been in the system to install the board driver, possible reasons for an error are:

- Board was removed
- Board driver did not start or was terminated
- PCI conflict after some other device was installed

Sapera comes with the following tools to help resolve PC2-Vision problems:

DALSA Log Viewer (**Start•Program•DALSA•Sapera LT•Tools•DALSA Log Viewer**): Lists various information and warning and error messages reported by DALSA boards (including the PC2-Vision driver).

PCI Diagnostics (**Start•Program•DALSA•Sapera LT•Tools•PCI Diagnostics**): Lists all PCI configuration space registers of the computer.

IFC comes with the following tools to help resolve PC2-Vision problems:

DALSA Log Viewer (**Start•Programs•IFC Version 5.8•Tools•DALSA Log Viewer**): Lists various information and warning and error messages reported by DALSA boards (including the PC2-Vision driver).

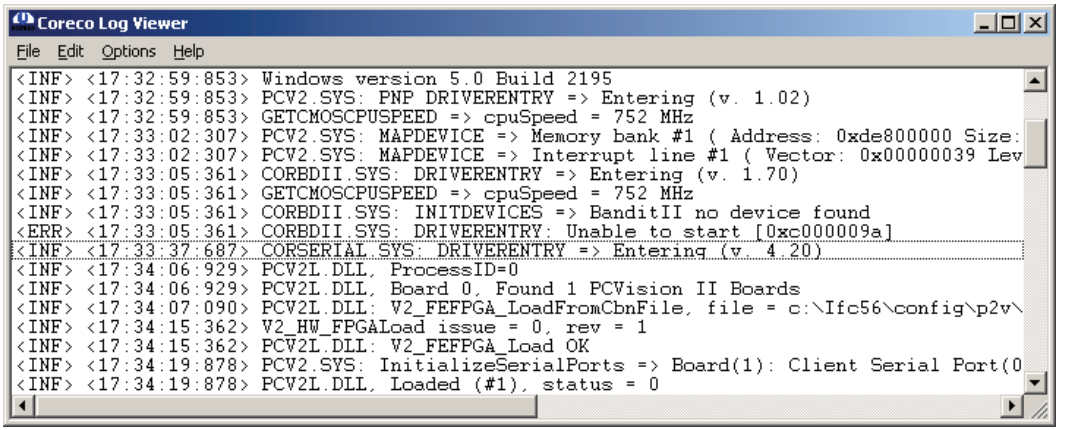
PCI Diagnostics (**Start•Programs•IFC Version 5.8•Tools•PCI Diagnostics**): Lists all PCI configuration space registers of the computer.

When you contact TELEDYNE DALSA Technical Support by e-mail, make certain that you attached two pieces of information (the log file and the pci dump file). They provide valuable information about your PC2-Vision to rapidly find the root cause of the problem.

Saving the Log

1. Start DALSA Log Viewer
2. Select menu "File / Save Messages…"
3. Select a filename (for example, **log.txt**)
4. Send log to DALSA Technical support

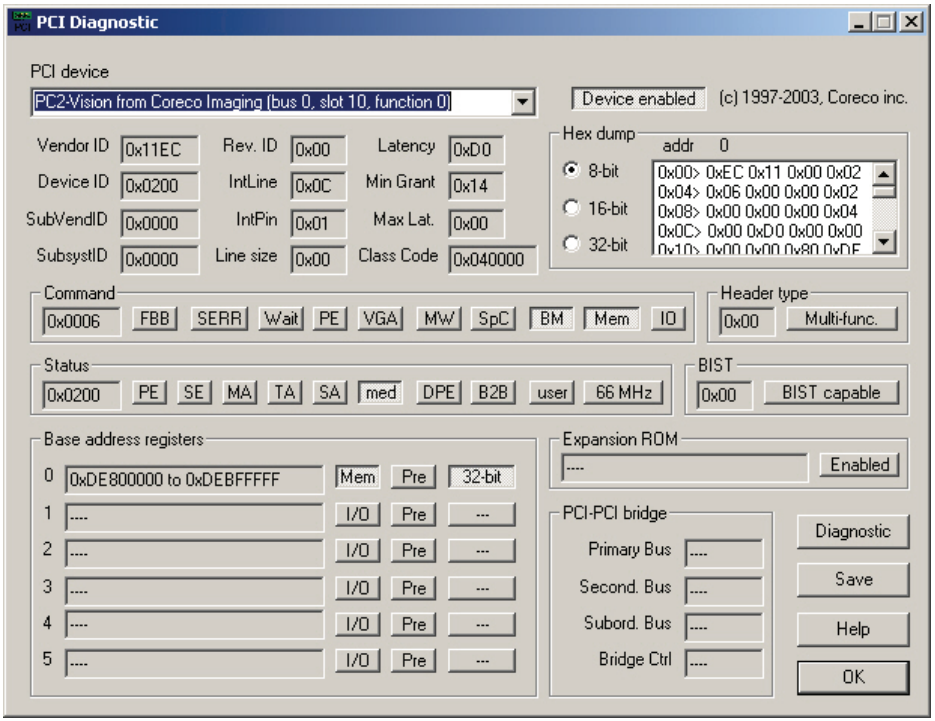
Below is a typical log:



Saving the PCI Diagnostics

1. Start PCI Diagnostics
2. Click the **Save** button. The dump of PCI configuration file is saved under **PCIDUMP.TXT**
3. Send **PCIDUMP.TXT** to DALSA Technical Support
4. Note DALSA PCI Vendor ID is 0x11EC. The PC2-Vision board PCI Device ID is 0x0200.

Below is a typical PCI configuration for a PC2-Vision:



Symptoms

PC2-Vision board not detected

The board is not seen when an application is started. This is due to a module creation error under IFC or because the Sapera Server is not present under Sapera.

Note: PC2-Vision is supported by two different APIs: Sapera LT and IFC. You must install one or the other. It is not possible for PC2-Vision to work under both APIs on the same machine. PC2-Vision will only work correctly with the last API installed on the machine. This ensures that the PC2-Vision driver matches the version of the API you are currently using.

This could stem from a hardware failure, a PCI problem, a plug and play problem, a kernel driver problem, or a software installation problem. You need to have 'administrator' privileges to install PC2-Vision software and to follow the troubleshooting guidelines given in this section.

Potential Hardware or PCI Failure

- Make certain that the PC2-Vision board is properly seated in the PCI slot. It is preferable to screw in the board securely to the computer chassis at the PCI bracket (some computer chassis use a clip mechanism instead of a screw). This ensures that the board remains stable when you connect/disconnect cables.
- Make certain that the 3.3V (LED1) or 5V (LED3) LED is lit at the back of the board (below the floppy power connector). If not, this indicates a problem with the PCI interface controller. Try a different PCI slot. This could also indicate a problem with the power supply provided by the PCI bus to the board.
- Make certain that the PC2-Vision is visible on the PCI bus. To do this, you can use the PCI diagnostic tools described above. Make certain that the PC2-Vision is displayed within the PCI device list. The DALSA PCI vendor ID is 0x11EC. The PC2-Vision PCI device ID is 0x0200. Ensure that a Base address register is assigned to PC2-Vision (lower left section of PCI Diagnostics). Ensure that the **Device Enable** button is activated (in the upper right section of PCI Diagnostics). If the board is not correctly mapped or activated, this may indicate a problem with the BIOS settings. You can go to your BIOS settings and check for PCI settings. The PCI slot number for PC2-Vision is reported by PCI Diagnostics. You can also try moving the board to a different PCI slot.

Potential Plug and Play or Driver Related Failure

After you have checked all the items in the preceding section you can proceed by validating that the board is correctly registered in Windows and that the associated kernel driver has started. Note that Windows NT® does not support plug and play.

- Start the DALSA Log Viewer tool. Check for '1 PC2-Vision device found' in the list of messages, as shown in bold below. If you do not see this, look for error messages (identified by <ERR> at the start of the line). Make certain that the memory is mapped successfully and that an interrupt line is assigned to the board. Ensure that the "VE_FEFPGA_Load OK" message is present. PC2-Vision driver related messages have the "**pcv2.sys**" string inserted before the actual message. If the DALSA Log indicates that the device is found, proceed to next section.

```
PCV2.SYS: DRIVERENTRY => Windows version 5.0 Build 2195 : M:\pc2\dev\pcv2\Driver\Kernel\Winnt
PCV2.SYS: DRIVERENTRY => Entering (v. 1.32) : M:\pc2\dev\pcv2\Driver\Kernel\Winnt\ms\board.c
GETCMOSCPUSPEED => cpuSpeed = 1752 MHz : M:\pc2\dev\pcv2\Driver\Kernel\Winnt\ms\cortime.c (85)
PCV2.SYS: DRIVERENTRY =>: Last installation is for Sapera: M:\pc2\dev\pcv2\Driver\Ke
PCV2.SYS: BOARDFINDDEVICE => Looking for PC2-Vision : M:\pc2\dev\pcv2\Driver\Kernel\Winnt\ms\
PCV2.SYS: INITBOARDEXTENSION => bus 0 slot 10  : M:\pc2\dev\pcv2\Driver\Kernel\Winnt\ms\board
PCV2.SYS: BOARDPARSERESOURCES => Memory bank #1 ( Address: 0xde000000 Size: 0x00400000) : M:\
PCV2.SYS: BOARDPARSERESOURCES => Interrupt line #1 ( Vector: 0x00000009 Level: 0x00000009) :
PCV2.SYS: BOARDPARSERESOURCES => Memory mapped successfully : M:\pc2\dev\pcv2\Driver\Kernel\W
PCV2.SYS: INITDEVICES => 1 PC2-Vision device found : M:\pc2\dev\pcv2\Driver\Kernel\Winnt\ms\b
PCV2L.DLL, ProcessID=0 : D:\pc2\dev\pcv2\Driver\User\pcv2api.c (367)
PCV2L.DLL, Board 0, Found 1 PC2-Vision Boards  : D:\pc2\dev\pcv2\Driver\User\pcv2api.c (453)
PCV2L.DLL: V2_FEFPGA_LoadFromCbnFile, file = C:\Ifc58\config\p2v\exo\pcv2.cbn : D:\pc2\dev\pc
V2_HW_FPGALoad issue = 0, rev = 2 : M:\pc2\dev\pcv2\Driver\Kernel\Winnt\ms\pcv2hw.c (152)
PCV2L.DLL: V2_FEFPGA_Load OK : D:\pc2\dev\pcv2\Driver\User\FEfpga.c (692)
PCV2.SYS: CorSerialAddDevice => CorSerial Interface Version: Board Driver:3, CorSerial:3 : M:
PCV2.SYS: CorSerialCreatePorts => Board(1): Client Serial Port(0) Created : M:\pc2\dev\pcv2\D
PCV2L.DLL: Power is OK on Power Connector (J6) : D:\pc2\dev\pcv2\Driver\User\FEfpga.c (711)
PCV2L.DLL, Loaded (#1), status = 0 : D:\pc2\dev\pcv2\Driver\User\pcv2api.c (981)
PCV2L.DLL, Unloaded (#1) : D:\pc2\dev\pcv2\Driver\User\pcv2api.c (986)
PCV2L.DLL, ProcessID=0 : D:\pc2\dev\pcv2\Driver\User\pcv2api.c (367)
PCV2L.DLL, Board 0, Found 1 PC2-Vision Boards  : D:\pc2\dev\pcv2\Driver\User\pcv2api.c (453)
PCV2L.DLL, Loaded (#1), status = 0 : D:\pc2\dev\pcv2\Driver\User\pcv2api.c (981)
```

- Open Windows Explorer to ensure that the **pcv2.sys** file is copied to your **Winnt\system32\drivers or Win\system32\drivers** folder. If it is not, this points to a software installation problem. You may try to uninstall and reinstall the software. Make certain that you have 'administrator' privileges when you perform installation. Follow all directives given by the installation program.
- Open the Registry editor. Click on Windows **Start** button and select 'Run…'. In the Run dialog box, type '`regedit`' (without the quotes) and click **OK**. This will start the registry editor. Go to the HKEY_LOCAL_MACHINE•SYSTEM•CurrentControlSet•Service•Pcv2 folder. You should see the following key:

    - Start
    - REG_DWORD
    - 0x00000002

- If the Pcv2 folder is absent, this indicates a problem with the installation process. Make certain that you have 'administrator' privileges when you perform installation.
- If the log does not show any indication that the PC2-Vision driver had started, you may have a plug and play problem. If you have Windows® 2000 or Windows® XP, go to **ControlPanel•System•Hardware•Device Manager**. Look for PC2-Vision under 'Imaging Devices'. Double-click and look at the device status. You should see: "This device is working properly". If this indication is not present, you may try to manually install the **.INF** file.

The **PCV2.INF** file is located in your PC2-Vision folder:

…**\DALSA\pc2-vision\win2000\inf\pc2c.inf**

The **PC2Vision.INF** file is located in:

…**\Ifc58\bin\win2000\pcvision.inf**

Open Windows Explorer and go to the **.INF** folder. Right-click on the **.INF** file and select **Install**. Note that this does not apply to Windows NT® .

Board does not grab

You are able to start Sapera CamExpert or IFC Camera Configurator®, but you do not see an image and the frame rate displayed is 0.

- If your camera is powered through a camera cable, make certain that J6 on the PC2-Vision is connected to a floppy power cable. Otherwise, the camera must be powered using an external power supply.
- Make certain that you provide an external trigger if the camera config file requires one. You can try generating a software trigger if you do not have a trigger source.
- Does your camera provide a WEN signal that you need to use? Adapt your config file and camera cable accordingly.
- Make certain that the pinout of your camera cable matches your camera and that the camera is properly connected to the cable.
- Make certain that the camera cable is plugged into J1 (upper MDR-36) for camera 1, 2 and 3, or in J2 (lower MDR-36) for camera 4, 5 and 6.
- Make certain that the camera is configured for the proper mode of operation (Composite Video, Separate Sync, Master Mode). This must match the camera config file. Refer to your camera datasheet.
- Try using a standard camera (RS-170 or CCIR) and select P2V_DEF_RS512x480P for RS-170 or P2V_DEF_CC512x512P for CCIR. This validates that PC2-Vision is able to grab and may point to a problem with your camera config file.
- In config file, make certain that you have the proper source of synchronization (Source of input sync parameter in Configurator®) for your camera.
- In the Configurator®, crop the image to 320 x 200 to make certain that enough pixels are sent by the camera to fill each line.
- Try creating a XTAL config file for your camera. This ensures that PC2-Vision boards see synchronization signals.
- Try to snap one frame from the Configurator® instead of continuous grab.
- Try using the SeqSnap demo to grab.
- Make certain an interrupt is assigned to the board in PCI Diagnostics. “IntLine” field holds a value different from 0.

Board grabs black

You are able to use Sapera CamExpert or IFC Camera Configurator®; the frame rate is as expected, but the display stays black.

- Try changing anti-aliasing filter selection (6MHz, 12MHz or bypass).
- Try changing Contrast/Brightness settings.
- Try changing the clamping setting (DC restoration).
- Make certain that the input LUT is not filled with '0's.
- Make certain that the iris of the lens on your camera is opened.
- This problem is sometimes caused by a PCI transfer issue. No PCI transfer takes place, so the frame rate is above 0 but nevertheless no image is displayed in Camera Configurator®. Under IFC, use IntrEx demo to see if you receive a P2V_INTR_BMDONE interrupt. Camera must be connected to port 0 and you need to have an appropriate **P2VTEST.TXT** file from Configurator®.
- Make certain that BUS MASTER bit in the PCI configuration space is activated. Look in PCI Diagnostics for **BM** button under "Command" group. Make certain that the **BM** button is activated.

Contact Information

Sales Information

Visit our web site: www.teledynedalsa.com/mv

Email: mailto:info@teledynedalsa.com

Canadian Sales

Teledyne DALSA — Head office
605 McMurray Road
Waterloo, Ontario, Canada, N2V 2E9

Tel: 519 886 6000
Fax: 519 886 8023

Teledyne DALSA — Montreal office
7075 Place Robert-Joncas, Suite #142
St. Laurent, Quebec, Canada, H4M 2Z2

Tel: (514) 333-1301
Fax: (514) 333-1388

USA Sales

Teledyne DALSA — Billerica office
700 Technology Park Drive
Billerica, Ma. 01821

Tel: (978) 670-2000
Fax: (978) 670-2010

European Sales

Teledyne DALSA GMBH
Felix-Wankel-Str. 1
82152 Krailling, Germany

Tel: +49 – 89 89 – 54 57 3-80
Fax: +49 – 89 89 – 54 57 3-46

Asian Sales

Teledyne DALSA Asia Pacific
Ikebukuro East 13F
3-4-3 Higashi Ikebukuro,
Toshima-ku, Tokyo, Japan

Tel: +81 3 5960 6353
Fax: +81 3 5960 6354

Shanghai Industrial Investment Building
Room G, 20F, 18 North Cao Xi Road,
Shanghai, China 200030

Tel: +86-21-64279081
Fax: +86-21-64699430

Technical Support

Any support question or request can be submitted via our web site:

Technical support form via our web page: Support requests for imaging product installations, Support requests for imaging applications	http://www.teledynedalsa.com/mv/support
Camera support information	
Product literature and driver updates	

Glossary of Terms

Bandwidth

Describes the measure of data transfer capacity. A computer system's PCI expansion bus is rated for a maximum peak data bandwidth of 132 MB/s. PCI devices must share the maximum PCI bus bandwidth when transferring data to and from system memory or other devices.

Bus

A common pathway, or channel, between multiple devices. Besides the computer's internal bus to memory and system components, peripheral buses such as PCI and AGP, allow adding or changing devices that make up the computer system.

Composite sync

Synchronization signals that combines the vertical component (video field or frame sync) with the horizontal component (video line sync). Often RGB cameras, besides the three color signals, have a fourth composite sync (CS) signal.

Composite Video

A video signal that is composed of the luminance and color information plus the synchronization signals together. Common composite video formats are NTSC and PAL.

Driver

Also called a device driver, a program routine that links a peripheral device to the operating system. Specific to the Bandit-II, its VGA driver is required for its display adapter functionality and a device driver is required for its frame grabber capabilities.

Frame

One complete image data set or its equivalent storage space.

Frame buffer

An area of memory used to hold a frame of image data. A frame buffer may exist on the acquisition hardware or be allocated by the acquisition hardware device driver in host system memory.

Grab

Acquiring an image frame by means of a frame grabber.

Grayscale

In image processing, the range of available brightness levels, displayed in shades of gray. In an 8-bit system, the gray scale contains values from 0 to 255.

Host

Refers to the computer system that supports the installed frame grabber.

Interlaced

Describing the standard television method of raster scanning in which the image is the product of two fields, each of which is made up of the image's alternate lines (that is, one field is comprised of lines 1, 3, 5, etc., and the other is comprised of lines 2, 4, 6, etc.)

Low-Pass Filter

A filter that blocks high frequencies and allows lower frequencies to pass through. Used to limit undesirable analog information (such as high frequency video noise) before converting to digital data.

MDR

Mini Delta Ribbon cable.

NTSC

National Television Systems Committee. Color TV standard used in North America and other countries. The interlaced video signal is composed of a total of 525 video lines at a frame rate of 30 Hz.

PAL

Phase Alteration by Line. Color TV standard used in most of Europe and other countries. The interlaced video signal is composed of a total of 625 video lines at a frame rate of 25 Hz.

PCI

Peripheral Component Interconnect. The PCI local bus is a 32-bit high performance expansion bus intended for interconnecting add-in boards, controllers, and processor/memory systems.

Pixel

A contraction of "picture element". The number of pixels describes the number of digital samples taken of the analog video signal. The number of pixels per video line by the number of active video lines describes the acquisition image resolution. The binary size of each pixel (for example, 8-bits, 15-bits, 24-bits) defines the number of gray levels or colors possible for each pixel.

RGB

A representation of color using the three primary colors (red, green, blue) as components. Video signals in RGB format are typically a non-composite video standard. A digital true color image can be represented by 8-bits per color (24-bits/pixel). Often image data is stored or transferred in 32-bits/pixel where the upper 8-bits of each pixel are unused.

Scatter-Gather

Host system memory allocated for frame buffers is virtually contiguous but physically scattered throughout all available memory.

TTL

Transistor-Transistor Logic. Acceptable TTL gate input signal voltage levels are:

LOW: lower than 0.8V

HIGH: higher than 2.0V

Any voltage between 0.8V and 2.0V is uncertain and will not be reliably interpreted by the TTL device.

Trigger

A mechanism that initiates an action when an event occurs such as synchronizing an image acquisition to an external event. A trigger generally causes a program routine to be executed such as the resetting of camera exposure and/or the firing of a strobe light.

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